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Sub-femto-Farad Resolution Electronic Interfaces for Integrated Capacitive Sensors: a Review

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ABSTRACT Capacitance detection is a universal transduction mechanism used in a wide variety of sensors and applications. It requires an electronic front-end converting the capacitance variation into another more convenient physical variable, ultimately determining the performance of the whole sensor. In this paper we present a comprehensive review of the different signal conditioning front-end topologies targeted in particular at sub-femtofarad resolution. Main design equations and analysis of the limits due to noise are reported in order to provide the designer with guidelines for choosing the most suitable topology according to the main design specifications, namely energy consumption, area occupation, measuring time and resolution. A data-driven comparison of the different solutions in literature is also carried out revealing that resolution, measuring time, area occupation and energy/conversion lower than 100 aF, 1 ms 0.1 mm^2, and 100 pJ/conv. can be obtained by capacitance to digital topologies, which therefore allow to get the best compromise among all design specifications.

INDEX TERMS Capacitance measurement, Capacitive sensors, Charge based capacitance measurement, Lock-In amplifier, Sigma-Delta modulator, Switched capacitor amplifier.

I. INTRODUCTION

Capacitive sensing is nowadays one of the most frequently adopted transduction methods in integrated electronic systems due to its relative simplicity of implementation, high sensitivity, high resolution, low temperature sensitivity and low noise performance [1]. Integrated capacitive sensors are widely employed in many applications such as gyroscopes [2], [3], accelerometers [3]–[6], humidity sensors [7], [8], displacement sensors [9] and biological sensors [10]–[15]. Since capacitive sensors can be designed to avoid static power consumption, they are also very suitable in low-power and energy-constrained applications, such as battery-powered systems, wireless sensor networks, and IoT systems [16], [17].

To measure a capacitance value and convert it into a variable that can be a voltage, a current, a frequency or a pulse width, an electronic interface is required whose specific readout architecture depends upon the system constraints, the main of which is the resolution, especially in applications where capacitance variations in the sub-femtofarad range must be detected. As an example, Fig. 1 shows two

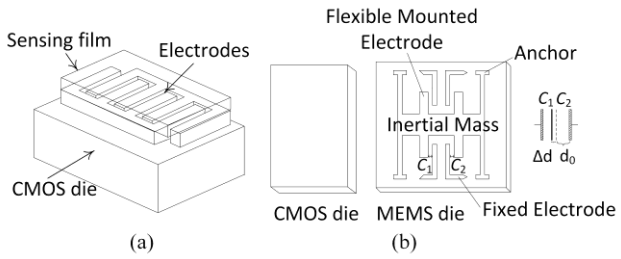

FIGURE 1. Examples of capacitive sensors: (a) humidity sensor; (b) accelerometer.

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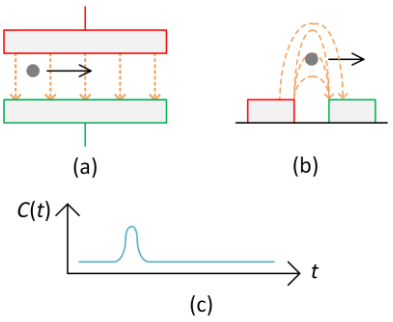

FIGURE 2. In-flow capacitive sensing of airborne particulate matter: (a) parallel-plate capacitor configuration; (b) planar capacitor configuration; (c) transient of the capacitance variation due to the particle flow

applications where a precise capacitive sensing is required, namely a humidity sensor and an accelerometer. In the first case (Fig. 1a), the sensor relies on the change of the permittivity of the sensing film (usually implemented with polymide) due to humidity, which in turn changes the fringe capacitance of the planar interdigitated capacitor in the range of few femtofarads. The readout electronics and the capacitive sensors are here implemented on the same die since the interdigitated capacitor is simply realized exploiting the upper metal level available in a standard CMOS technology [8]. On the other hand, the accelerometer in Fig. 1b relies on the movement of the inertial mass that changes the distance between the plates of the capacitor, thus producing a capacitance variation as low as few attofarads [1], [4]. This variation is detected by the electronic front-end which in this case is placed on a second die, bonded to the first one at the package level since the MEMS (micro electro-mechanical systems) process used to implement the inertial mass is not compatible with the CMOS technology.

The measuring time of the sensor (alternatively specified in terms of bandwidth) is another important performance parameter of the electronic interface. Usually, a measuring time in the order of milliseconds is acceptable for humidity sensors, accelerometers and gyroscopes [3], [6], [8]. However, there are other applications where a much lower measuring time is required, such as in-flow capacitive sensors. Fig. 2 shows such an example in which capacitive sensing is exploited to implement an airborne particle matter detector [18]–[23]. Specifically, Fig. 2a shows a parallel-plate capacitor, in which the particle flows between the electrodes, while Fig. 2b depicts a planar configuration, in which the particle flows above the electrodes. In both cases, when the particle flows in the sensing capacitor, it produces a temporary capacitance variation due to the interaction with the electric field between the electrodes, as illustrated in Fig. 2c. The duration of the capacitance variation is a function of the particle speed and can be as low as few microseconds, thus requiring a high-speed electronic front-end.

Given the importance and widespread diffusion of integrated capacitive sensors, it is quite understandable that many different electronic interfaces have been presented in the open literature. Purpose of this paper is to provide a comprehensive review of these readout implementations while deriving some guidelines for choosing a specific solution according to the design specifications. More specifically, a data-driven comparison of the state-of-art is presented which offers additional hints to the designer in the selection of the most suitable topology, with emphasis on applications requiring sub-femtofarad resolution.

II. CAPACITANCE TO VOLTAGE TOPOLOGIES

Capacitance to voltage (C2V) electronic front-ends provide conversion of the capacitance variation into an analog voltage that can be subsequently converted in the digital domain. There are three main approaches to implement a C2V conversion, namely charge sensitive amplifier, lock-in detection and charge-based capacitance measurement. These methods are discussed below. For the sake of simplicity, the single-ended version of the various topologies is considered, but the discussion can be readily applied also to the fully differential cases.

A. CHARGE SENSITIVE AMPLIFIER

Charge sensitive amplifier (CSA) method allows to convert a capacitance variation directly into a voltage through the use of a charge sensitive amplifier [6], [24]–[28]. Although continuous-time amplifiers can be in principle adopted, switched-capacitor topologies are usually preferred [29]. The principle of operation is shown in Fig. 3[1]. A voltage pulse, V_a, is applied to the sensing capacitor, C_x, while a voltage pulse of opposite value, V_a, is applied to the reference capacitor, C_{ref}[2]. Consequently, a charge proportional to the difference between C_x and C_{ref}, ΔC_x, is integrated on the feedback capacitor, C_f.

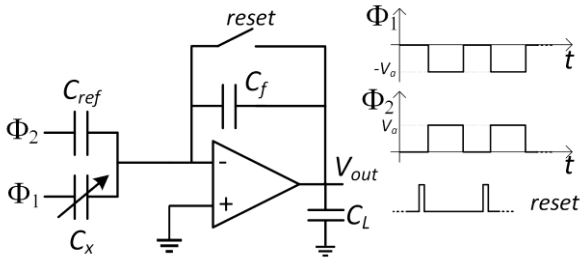

FIGURE 3. *Capacitance to voltage topology based on charge sensitive amplifier*

[1] Fig. 3 refers to a half-bridge configuration which is suitable for single ended sense capacitors, like the case of the humidity sensor in Fig. 1a. A full-bridge configuration with a fully differential amplifier can be formed as well for a differential sense-capacitor, like that of the accelerometer in Fig. 1b.

[2] The reference capacitor is set equal to the rest sense capacitance. Note, moreover, that the in Fig. 3 a dual supply is assumed for the amplifer and, consequently, the virtual ground node at the noninverting input is equal to zero.

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The output voltage during the time intervals where Φ_1 and Φ_2 are nonzero is therefore is given by

$$V_{out} = \frac{C_x - C_{ref}}{C_f} V_a = \frac{\Delta C_x}{C_f} V_a \quad (1)$$

The reset switch prevents saturation of the amplifier output. Charge injection and offsets are some problems added by the switches of switched capacitor circuits. Double sampling and auto-zeroing methods are some of the most useful approaches to reduce the imperfections of these kind of circuits [25]-[32].

The minimum detectable capacitance variation can be defined considering the signal-to-noise (*SNR*) ratio and evaluating the signal whose amplitude is equal to the noise root-mean-square. Assuming that the amplifier is implemented by a single-stage OTA with unity-gain bandwidth equal to g_m/C_L, the *SNR* is evaluated in [26] as

$$SNR = \frac{\beta\left[C_L + (1-\beta)C_f\right]}{4kTC_f\left[C_L + (1-\beta+\alpha\gamma)C_f\right]}\left(\Delta C_x V_a\right)^2 \quad (2)$$

where k is the Boltzmann constant, T is the absolute temperature, γ is the noise coefficient of MOS transistors, α is the topology-dependent excess noise factor of the amplifier and β is the feedback factor equal to $C_f/(C_x+C_{ref}+C_f)$[3]. By inspection of (2) it is apparent that the *SNR* can be increased by increasing the value of the amplitude of the excitation signal, V_a. The maximum value of V_a can be even higher than the supply voltage if proper DC-DC switching circuit are adopted (e.g., charge pumps), provided that it is compatible with the maximum voltage that the capacitors can withstand. Increasing the value of C_L also has a positive effect (because the equivalent noise bandwidth is reduced) but this comes at the expense of a reducing of the amplifier bandwidth. Another important design parameter is represented by the feedback capacitor value. In particular, reducing the value of C_f allows increasing the *SNR*. The minimum value of C_f is actually limited by parasitic capacitance which depends on the adopted technology, transistor dimensions of the amplifier input stage and layout strategy.

B. LOCK-IN DETECTION

The lock-in topology is one of the best technique to reduce the effect of noise and improve the resolution [13], [18], [19], [21]–[23], [30]. This technique is widely used in applications where the level of the signal is comparable to that of noise.

Fig. 4 shows the simplified single-ended version of a read-out circuit based on the lock-in technique [30]. Parameter Z_x represents the impedance of the sensing electrode which is driven by a sinusoidal signal with amplitude V_{AC} and frequency f_{AC}, generated through an excitation signal generator[4]. The current flowing in Z_x is converted into a voltage by a transimpedance amplifier (TIA) and then processed by the lock-in demodulator (LID) which is made up by two multipliers and two tunable low-pass filters. Each multiplier shifts the signal from f_{AC} to DC while the filter removes the replica of the spectrum around $2f_{AC}$. Being synchronized with the excitation signal V_{AC}, the LID can extract the in-phase (Re[Z]) and in-quadrature (Im[Z]) components of Z_x.

As demonstrated in [20], assuming that impedance Z_x as purely capacitive and neglecting the noise of the excitation signal generator, the *SNR* of the circuit in Fig. 4 can be assumed to be proportional to

$$SNR \propto \frac{g_m\left(\Delta C_x V_{AC}\right)^2}{4kT\left(C_x + C_{par}\right)^2 ENBW} \quad (3)$$

where C_{par} is defined in Fig.4, k is the Boltzmann constant, T is the absolute temperature, *ENBW* is the equivalent noise bandwidth of the circuit which is actually set by the corner frequency of the low-pass filter[5]. This filter allows to remove the high frequency replicas of the signal which also contains the upconverted low-frequency noise (flicker noise). It is apparent from (3) that the *SNR* can be increased, apart by increasing V_{AC}, by reducing the bandwidth of the circuit and reducing the rest value of the sensing capacitor, Z_x and the associated parasitic capacitance. While the value of C_x is basically proportional to the area of the integrated capacitor and is strictly related to the specific application, the value of C_x can be reduced by subdividing the sensing capacitor into smaller capacitors that are serially processed through a multiplexer [22]. To reduce the parasitic arising from the coupling of capacitor C_x to the substrate, the highest available metal levels should be adopted to implement the sensing capacitor.

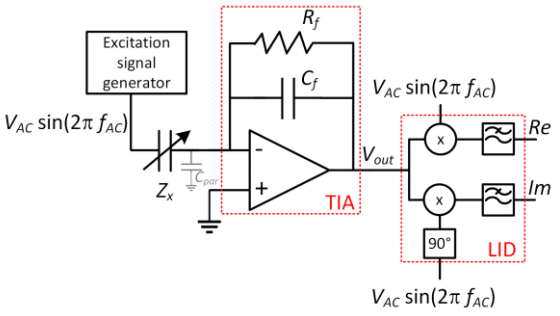

FIGURE 4. ***Capacitance to voltage topology based on lock-in detection.***

[3] A more precise equation for the feedback factor considers the parasitic capacitance at the input node of the amplifier [26].

[4] It should be noted that a square-wave signal can be used as well to simplify the design of the excitation signal generator [19], [30].

[5] The filter corner frequency is set according to the bandwidth of the monitored signal (usually much lower than f_{AC}). Note, moreover, that the filter may be band-pass to remove the very low frequencies, if they are not of interest.

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Thanks to the connection of one terminal of Z_x to virtual ground, the voltage across the sensing impedance can be accurately controlled by setting the amplitude of V_{AC} through the excitation signal generator. This amplitude is usually set to the highest value in order to maximize *SNR*. However, in electrochemical and biological applications, where cells and macromolecules are very sensitive to the applied field and potential, the maximum value for V_{AC} cannot be used to maximize the *SNR* and a tight control of the excitation voltage amplitude is mandatory [30].

Moreover, the connection of one terminal of Z_x to virtual ground allows us to neutralize the effects of the parasitic capacitance, C_{par}. which is connected between virtual ground and ground. Being always discharged, C_{par} does not influence the operation of the amplifier.

Whenever possible, a differential configuration is advisable. It requires a second reference impedance connected in a similar fashion as in Fig. 3 [30]. This scheme allows to improve the dynamic range, since only the current difference is amplified, and to reject the noise from V_{AC} and any other common-mode noise picked up by the reference and sensing impedance. However, this approach requires additional circuitry in the excitation signal block (which causes additional noise) and leads to doubling the value of C_x in (3), thus reducing the *SNR*.

The main limitation of the lock-in technique is due to the TIA which is affected by a resolution/speed trade-off. Indeed, since the noise current power spectral density is equal to $4kT/R_f$, where k is the Boltzmann constant and T is the absolute temperature, to achieve a low thermal noise the value of R_f should be maximized. On the other hand, the TIA bandwidth is limited by the pole $\omega_p=(2\pi C_f R_f)^{-1}$, thus requiring smaller R_f to obtain wide bandwidth. Consequently, a trade-off in the value of the feedback resistor R_f must be achieved to get a balance among the different specifications [31]-[33].

The main limit of this method is its ability to detect only slow capacitance variations.

C. CHARGE-BASED CAPACITANCE MEASUREMENT

Charge-based capacitance measurement (CBCM) was originally proposed in [34] for on-chip measurement of sub-femtofarad interconnect capacitances. Thanks to its high resolution, this method can be used in those applications where the capacitance variation is down to few attofarads [35]-[44]. Fig. 5 shows a basic circuit that exploits the CBCM approach [44]. Capacitors C_x and C_{ref} are the sensing capacitor and reference capacitor, respectively, which are driven by four switches implemented by transistors M1-M4. When clock phases Φ_1 and Φ_2 are low, C_x and C_{ref} are charged through transistors M3 and M4 and when these two clocks phases are high, the capacitors are discharged via M1 and M2. Observe that Φ_1 and Φ_2 are set to avoid short-circuit current from V_{DD} to ground, i.e. concurrent activation of transistors M1-M3 and M2-M4. Current mirrors M5-M7, M6-M8 and M9-M10 enable subtraction of the instantaneous currents flowing in C_x and C_{ref}, yielding

$$i_x(t) = m\left(C_x\frac{dv}{dt} - C_{ref}\frac{dv}{dt}\right) \tag{4}$$

where m is the gain of the current mirrors. The current difference i_x is then averaged using the integrating capacitor C_{int}. Integrating over one clock period, T_S, yields [44]

$$\int_0^{T_S} i_x(t)dt = \int_0^{V_C} m\left(C_x\frac{dv}{dt} - C_{ref}\frac{dv}{dt}\right)dt \approx m\left(V_{DD}-V_{TH}\right)\Delta C_x \tag{5}$$

where the rightmost approximation holds considering that C_x and C_{ref} are charged to nearly V_{DD}-V_{TH} in one clock period, being V_{TH} the threshold voltage of transistors M5 and M6. The voltage across C_{int} is then given by

$$V_{out} \approx m\left(V_{DD}-V_{TH}\right)\frac{\Delta C_x}{C_{\text{int}}} \tag{6}$$

It is apparent that V_{out} is proportional to ΔC_x, m and (V_{DD}-V_{TH}) and is inversely proportional C_{int}.

The accuracy of the CBCM topology is actually limited by mismatches between the two branches that can be compensated by adopting a careful layout style and using accurate current mirror topologies. Moreover, trimming and compensation schemes can be adopted as well to improve accuracy [37].

Charge injection phenomena represent another limiting factor of the accuracy of the CBCM topology. This issue, as well known, can be alleviated by adopting transmission gates to implement the switches. Dummy switches can be also exploited to strongly mitigate charge injection mismatches [42].

The minimum detectable capacitance variation ΔC is actually limited by noise. Using (6) and neglecting the noise introduced by the current mirrors, the *SNR* can be assumed to be proportional to

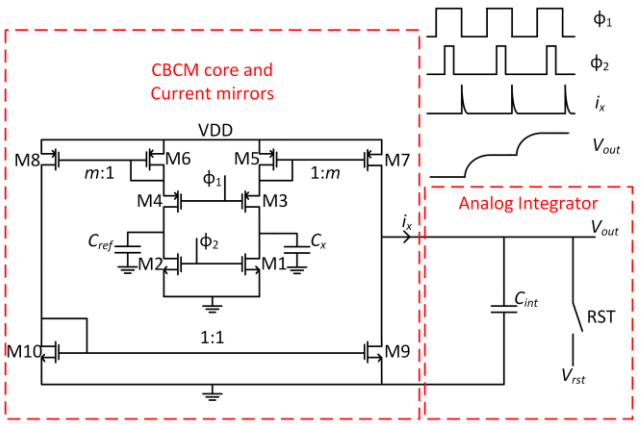

FIGURE 5. ***Capacitance to voltage topology based on charge based capacitance measurement circuit (adapted from [44]).***

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$$SNR \propto \frac{\left(\frac{V_{out}}{\sqrt{2}}\right)^2}{v_{noise,rms}^2} = \frac{m^2 \Delta C_x^2 \left(V_{DD} - V_{TH}\right)^2}{4kTC_{\text{int}}} \left(\frac{C_x}{C_{\text{int}}}\right) \quad (7)$$

where the noise of CBCM core is evaluated as the thermal noise of a conventional switched capacitor circuit. By inspection of (7) it is apparent that the *SNR*, is improved by reducing the value of C_{int}, increasing the current mirror gain and the overdrive voltage. Optimal choice of these parameters can lead to resolution values down to the attofarad range [37].

III. CAPACITANCE TO CURRENT TOPOLOGIES

Capacitance to current (C2I) techniques could be profitably adopted to increase speed as well as to simplify the circuit complexity and enable low-voltage low-power operation [45]–[47]. The principle of operation is shown in Fig. 6, where sensing and reference capacitors, C_x and C_{ref}, are connected to a current-differencing block providing input virtual ground [45]. A constant current, I_a, supplies the common node of C_x and C_{ref} capacitors. C_{stray} models the parasitic capacitance to ground, given by the input sensor capacitance, that of the switches and that of the current reference. Since the use of a constant current would cause a linear increase of the voltage at the sensor common node, two switches periodically discharging C_{ref} and C_x are included to avoid the saturation of the circuit. Switches are controlled by a clocked signal of period T equal to T_D+T_M. During the discharge phase (T_D) S_1 and S_2 are closed and currents i_1 and i_2 become both equal, thereby forcing i_{out} to be zero. In contrast, during the measure phase (T_M), the expression of the output current is proportional to C_x–C_{ref}

$$i_{out} = i_1 - i_2 = I_a \frac{C_x - C_{ref}}{C_x + C_{ref} + C_{stray}} \quad (8)$$

The presence of C_x in the denominator of (8) causes an error that is ideally eliminated if $C_x + C_{ref}$ is constant. This occurs in differential capacitive sensors, where both C_x and C_{ref} vary of the same quantity, ΔC_x, but with opposite signs [45], [46]. In this way, $C_x+C_{ref} = 2C_{ref}$ and $C_x-C_{ref}=2\Delta C_x$. Thus, the output current is directly proportional to the capacitive variation.

As a main drawback, the output current is sensitive to the sensor stray capacitance which can be reduced by implementing the sensing and reference capacitor on chip and by adopting proper layout strategies. In particular, it is advisable to use the highest possible metal level to reduce coupling with the substrate.

To get rid of C_{stray}, the solution proposed in [46] can be adopted, which employs a signal-processing block with both current-summing and current-differencing capability. By exploiting an autotuning feedback loop to control the common-mode current, virtually the same maximum sensitivity and measure accuracy irrespectively of the input stray capacitance is achieved.

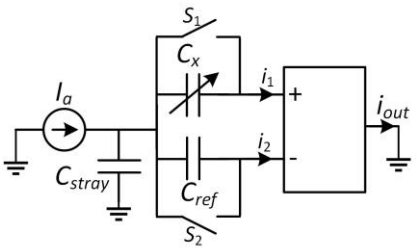

FIGURE 6. ***Scheme of the capacitance to current topology proposed in [48].***

The *SNR* is can be expressed as

$$SNR = \frac{\left(\frac{i_{out}}{\sqrt{2}}\right)^2}{i_{noise,rms}^2} \quad (9)$$

where i_{noise} is the equivalent noise current at the output of the differencing block. From (8) and (9) it is apparent that increasing the value of I_a allows increasing the *SNR*. The maximum allowable value of I_a is actually limited by the voltage induced during the measure phase at the sensor common node [46]. The equivalent noise output current is inversely proportional to the total bias current used of the differencing block. If the stray-insensitive topology is adopted [46], it can be concluded that the *SNR* is independent of the nominal value of C_x, unlike the C2V solutions in Section II, and it can be improved only by increasing the current (and area) consumption.

IV. CAPACITANCE TO FREQUENCY TOPOLOGIES

Capacitance to frequency (C2F) conversion is usually obtained through a ring oscillator [7], [14], [48]–[54]. Fig. 7a shows the principle of operation of this method. The sensing capacitor, C_x, is included as load of one inverter stage of the ring oscillator. The period of the output signal is then given by [51]

$$T_{out} = \frac{2V_{DD}}{I_{avg}} \left[C_x + \left(N - 1\right) C_{load} \right] \quad (10)$$

where C_{load} is the load capacitance of each stage, C_x is the sensing capacitance, N is the number of stages, V_{DD} is the supply voltage and I_{avg} is the average charging/discharging current of each stage, respectively. A variant of the basic topology is obtained by adopting current starved inverters to limit the maximum current consumption, as depicted in Fig. 7b. In this case the oscillation period is given by (10) with $I_{avg}=I_B$ and V_{DD} is V_{TH} [7], [14].

One of the advantages of this topology is that the output signal can be digitally converted by a simple counter.

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Moreover, the fully-digital architecture allows operation under very-low supply voltage.

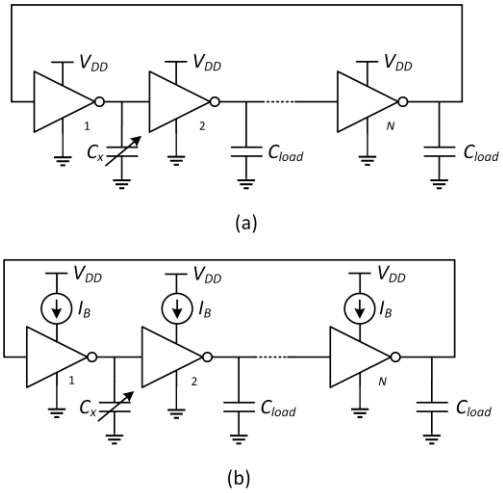

FIGURE 7. ***Ring oscillator-based capacitance to frequency converter: (a) standard; (b) current starved.***

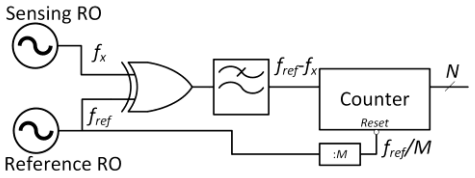

FIGURE 8. ***Differential ring oscillator-based capacitance to frequency converter.***

The maximum *SNR* of C2F topology of Fig. 7a is obtained in [52] by evaluating the ratio between the signal power[6] and the minimum jitter variance of the ring oscillator as

$$SNR = \frac{\left(\Delta C_x V_{DD}\right)^2}{3.67kT\left(C_x + \left(N-1\right)C_{load}\right)} \tag{11}$$

It can be noted that the *SNR* increases quadratically with the supply voltage. Moreover, reducing the value of C_x and C_{load} (i.e., increasing the oscillation frequency) has a positive effect on *SNR*. Since C_{load} is ultimately due to parasitic capacitors of the inverters, the *SNR* is limited by the adopted technology. Finally, using the minimum value for *N* (i.e., 3) improves also the *SNR*.

Single-ended ring oscillators are very susceptible to supply and substrate noise and this can have a huge impact on the phase noise performance. For this reason, a differential structure is advisable [51].

A drawback of solutions in Fig. 7 is the high sensitivity to environmental variations and temperature. To get rid of this drawback, a differential measure method exploiting two separate ring oscillators can be used to neutralize every common-mode disturbance, as shown in Fig. 8 [50], [53], [54]. The first oscillator is the sensing one while the second acts as reference. The difference between the output frequency of the two circuits is proportional to C_x-C_{load} and can be detected through a XOR gate and a low pass filter. Finally, a ripple counter is adopted which is reset through the clock generated by the reference oscillator divided by *M*. The number of counts at the output of the counter can be simply obtained by multiplying the frequency of the filter by the reset period of the counter, thus yielding

$$Counts = \left(f_{ref} - f_x\right)\frac{M}{f_{ref}} \tag{12}$$

where f_x the frequency of the sensing oscillator given by the inverse of (10), and f_{ref} is to the frequency of the reference oscillator given by the inverse of (10) for C_x=C_{load}. From (12) it is apparent that the counts depends on the ratio between f_x and f_{ref} and, consequently, the dependence on supply voltage and average current (and then temperature) is eliminated.

V. CAPACITANCE TO TIME TOPOLOGY

Interfaces based on capacitance to time (C2T) conversion are basically relaxation oscillators converting the sensor capacitance into a time period, which can then be easily digitized using a counter [16], [55]–[58]. The principle of operation of C2T topology is shown in Fig. 9. A current reference, I_B, is exploited for charging the sensing capacitor, C_x. When the charging voltage reaches the reference voltage, V_{ref}, the comparator output goes high and the voltage of C_x is set to zero through transistor Ms. The output pulse period can be therefore expressed as

$$T_{out} = \frac{C_x V_{ref}}{I_B} + \tau_d \tag{13}$$

where τ_d is the delay introduced by the comparator.

Comparator-based relaxation oscillators need accurate current references and comparators. Furthermore, the output frequency of these sensors is dependent on parasitic capacitances and other parameters of the circuit such as the transistor threshold voltage, which are variable with temperature and process [15]. To get rid of some of these drawbacks, more complex topologies have been proposed in [59]-[61].

[6] The signal power is evaluated from (10) as $\Delta T_{out,rms}^2 = \left(\frac{\Delta T}{\sqrt{2}}\right)^2 = \frac{2\left(\Delta C_x V_{DD}\right)^2}{I_{avg}^2}$

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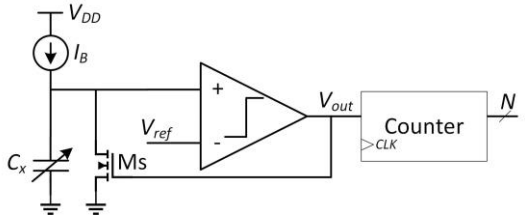

FIGURE 9. ***Capacitance to time topology based on relaxation oscillator.***

The minimum detectable sensing capacitance is affected by the noise generated by the interface circuit, namely the comparator and the reference voltage generator. Neglecting the propagation delay of the comparator, the *SNR* can be evaluated by the ratio between the signal power and the time deviation due to jitter as

$$SNR = \frac{\left(\frac{\Delta T}{\sqrt{2}}\right)^2}{\sigma_j^2} = \frac{\left(\Delta C_x V_{ref}\right)^2}{I_B^2\left(\sigma_{comp}^2 + \sigma_{Vref}^2\right)} \qquad (14)$$

where are the jitter variance of the comparator and the voltage reference which are assumed to have a Gaussian distribution. Analysis of (14) reveals that *SNR* is improved by prolonging the time to charge C_x through a reduction of I_B or by increasing the reference voltage value of the comparator. This latter option is however limited by the power supply voltage and the input dynamic range of the comparator.

VI. CAPACITANCE TO DIGITAL TOPOLOGIES

In order to obtain a digital output, C2V interfaces have to be combined with an analog to digital converter, involving extra power and complexity [3], [8], [9], [14], [27]–[29], [62]–[72]. Capacitance to digital (C2D) topologies allow direct digitization of the sensor capacitance without performing intermediate C2V conversion.

A. SIGMA-DELTA METHOD

A widely adopted method to implement C2D conversion exploits ΣΔ modulators [8], [27], [64], [68]-[72]. These topologies can achieve high signal to noise ratios due to oversampling and noise-shaping properties.

An example of CDC topology is reported in [8] where a humidity-sensitive capacitance variation is digitized though the circuit shown in Fig. 10a. The circuit relies on a third-order delta-sigma modulator, illustrated in Fig. 10b. After an initial reset of the integrator, a charge proportional to C_x-C_{off} is integrated in every clock cycle of the conversion, in addition to a charge proportional to C_{ref} with a polarity that depends on the bit-stream output. The negative feedback in the modulator ensures that the latter, resulting in a zero average charge flowing into the loop filter, balances the former charge, resulting in a zero average charge flowing into the loop filter

$$C_x - C_{off} - \mu C_{ref} + (1-\mu)C_{ref} = 0 \qquad (15)$$

where μ is the probability density of the bit stream, *bs*, comprised between 0 and 1.

A tradeoff between power consumption and resolution must be achieved. To obtain an energy-optimized CDC, the oversampling ratio, i.e., the number of clock cycles required to produce a digital output, should be minimized. However, based on results in [71], a high value of the oversampling ratio is required to obtain a proper noise rejection. Consequently, an optimum value for the oversampling ratio exists which allows to bring the thermal noise of the ΣΔ modulator to a level compatible with the target resolution while minimizing energy consumption.

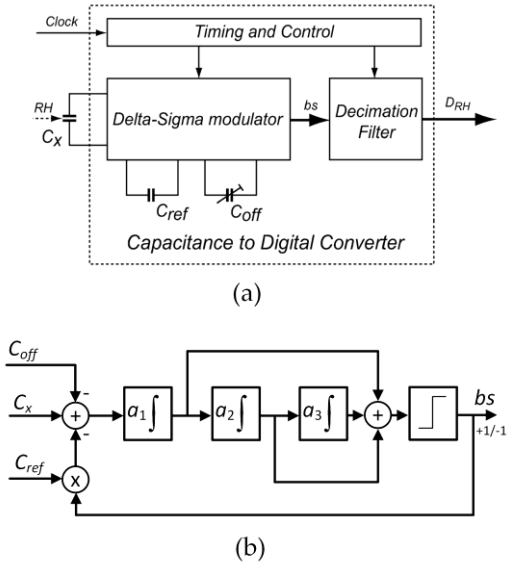

FIGURE 10. ***Capacitance to digital topology based on ΔΣ modulator [8]*: (a) block diagram; (b) schematic of the ΣΔ modulator.**

B. SAR METHOD

To avoid oversampling, a simple but effective capacitance-to-digital converter that relies on a successive approximation register (SAR) architecture was proposed in [65] and recently exploited in [26] and [72]. The SAR CDC is illustrated in Fig. 11 which includes the sensing capacitor, C_x, a Miller integrator (differential amplifier and C_F) with discharging MOS switch, a voltage comparator, a programmable capacitor array (PCA) implementing a reference capacitor, C_{ref}, a SAR logic block and two NOT gates driven by complementary nonoverlapped clock phases Φ_1 and Φ_2. The working principle is divided into two phases: the former is the precharge phase in which Φ_1 is high, C_x is discharged and the amplifier works as a buffer and sets V_X equal to V_{ref}. In this way, the total charge in C_x is given by $Q=C_xV_{ref}$. In the evaluation phase, Φ_1 is low and Φ_2 is high and the voltage difference across the sensing capacitor is 0 V. Consequently, the charge redistributes through C_{ref} and C_F and is given by

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$Q=C_{ref}V_{ref}+(V_{ref}-V_o)C_F$. As the charge is conserved, combining the two formulas we obtain

$$V_o = V_{ref} + V_{ref}\frac{C_{ref}-C_x}{C_F} \tag{16}$$

Thus, the differential input of the comparator is given by

$$\Delta V_o = V_o - V_{ref} = V_{ref}\frac{\Delta C_x}{C_F} \tag{17}$$

and the output of the comparator, V_{CMP}, is then equal to digital 0 or 1 when $C_{ref} > C_x$ and $C_{ref} < C_x$, respectively. Based on V_{CMP}, the SAR logic changes the PCA digital input to increase or decrease C_{ref}, using a binary search successive approximation algorithm. It is worth noting that any variation or drift of the reference voltage, V_{ref}, equally affects both the amplifier and the comparator and thus is cancelled.

Finally observe that the effects of the parasitic capacitances of C_x and C_{ref} can be neglected. Indeed, C_x and C_{ref} are either connected to ground, to V_{ref} or to the differential amplifier inverting input (that is virtually equal to V_{ref}) which are all low-impedance nodes[7]. Specifically, since potential V_x is virtually constant, the parasitic capacitors do not participate in charge redistribution and, consequently, they do not affect circuit operation.

The above analysis assumes ideal operation of the amplifier and the comparator and the SAR logic. A detailed analysis of errors due to process mismatch is reported in [65] and reveals that the offset voltage of the amplifier and the comparator introduce a limit to the minimum voltage variation that can be revealed.

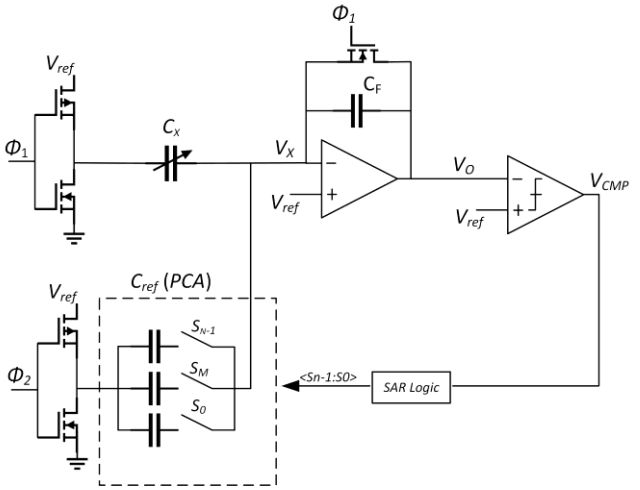

FIGURE 11. ***SAR Capacitance-to-Digital Converter.***

VII. COMPARISON

A comparison among different topologies reported in the literature and showing experimental sub-femtofarad resolution is reported in Table 1.

The best resolution, equal to 65 zF, is achieved by the lock-in topology reported in [22]. However, as highlighted in Section 2.2, this solution requires a relatively high power consumption and area occupation as compared to the other alternative topologies. On the other hand, the lowest power consumption is achieved by the solution reported in [8] and [62] based on C2D, ΣΔ and C2T topologies, respectively, which however are also among the circuits with the lowest supply voltage. The solution reported in [46] based on C2I topology shows the shortest measuring time. However, the resolution value is among the worst.

To carry out a quantitative comparison that takes into account several performance parameters at the same time, we adopt the figure of merit (FoM)[8] [8], [64], [69], [72]

$$FoM = \frac{Power \cdot Measuring\ time}{2^{(SNRcap-1.76)/6.02}} \tag{18}$$

where

$$SNRcap = 20Log\left(\frac{Range/2\sqrt{2}}{Resolution}\right) \tag{19}$$

and where *Range* represents the difference between the maximum and minimum measured capacitance while *Resolution* is the root mean square value of the minimum effective capacitance variation.

The *FoM* values are reported against resolution, measuring time, area, and power consumption in Figs. 12, 13, 14 and 15, respectively.

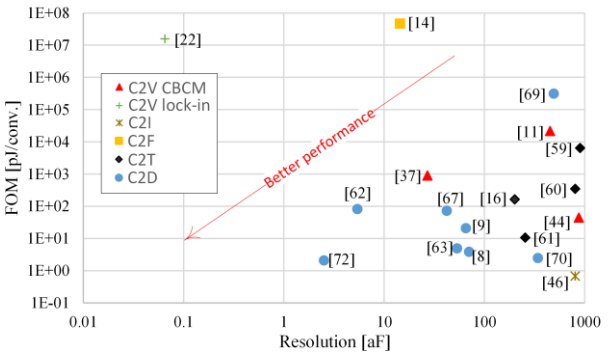

FIGURE 12. ***FOM defined in equation (18) versus resolution.***

[7] The inverting input exhibits low impedance thanks to the effect of negative feedback.

[8] FoM in (18) is defined assuming a sine-wave signal.

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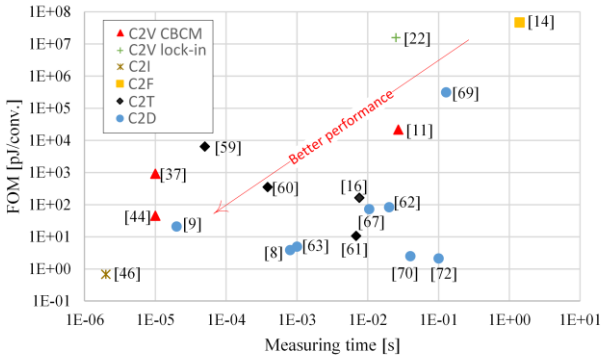

FIGURE 13. *FOM defined in equation (18) versus measuring time.*

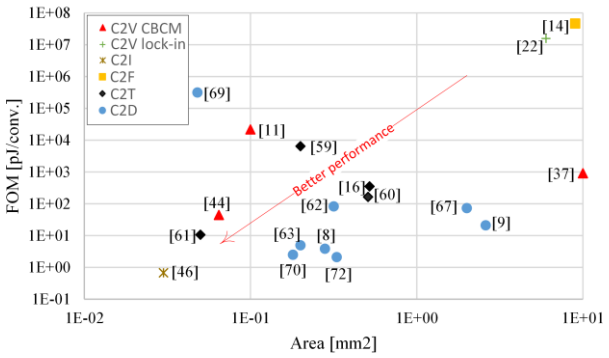

FIGURE 14. *FOM defined in equation (18) versus area occupation.*

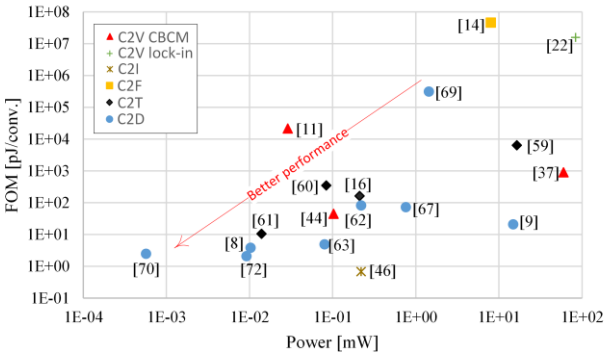

FIGURE 15. *FOM defined in equation (18) versus power consumption*

By inspection of Fig. 12 it is apparent that solutions [8], [9], [62], [63], [67] and [72], all based on C2D topology, achieve *FoM* values lower than 100 with a resolution lower than 100 aF. Among these solutions, [8], [9] and [67] are based on the ΣΔ architecture. Solution [8], [9] and [67] still exhibit a good speed performance, as apparent from Fig. 13, being their measuring time lower than 1 ms. However, also solution [44] and [46], respectively based on C2V CBCM and C2I topology, show a value of the *FoM* lower than 100 and measuring time lower than 1 ms. The good performance of [44] and [46] is still confirmed in Fig. 14, being their area occupation lower than 0.1 mm^2. Solutions reported in [61], based on C2T topology, is the only other one showing such a low area occupation performance. Note, however, that C2D solutions [8], [62], [63] and [70] still exhibit a relatively low

TABLE I
COMPARISON OF ELECTRONIC INTERFACES FOR INTEGRATED CAPACITIVE SENSORS WITH SUB-FEMTO-FARAD RESOLUTION

Ref.	topology	output	Tech. [nm]	Supply [V]	Power [mW]	Meas. Time [ms]	Range [pF]	Area [mm^2]	Resolution [aF]	Sensitivity
[8]	C2D SD	digital	160	1.2	0.01	0.8	0.52	0.28	70	-
[9]	C2D SD	digital	350	3.3	14.85	0.02	3.2	2.6	65	-
[11]	CBCM	analog	250	2.5	0.03	27	0.056	0.1	450	55 mV/fF
[14]	C2F RO	digital	350	3.3	8	1400	0.012	9	14.4	590 kHz/fF
[16]	C2T	semi-digital	350	3.3	0.21	7.6	6.8	0.51	200	-
[22]	C2V lock-in	analog	350	3.3	84	25	$3 \cdot 10^{-5}$	6	0.065	-
[27]	C2V + SD	digital	180	1.8	0.35	-	0.145	0.15	54	20 mV/fF
[37]	CBCM	analog	130	2.5	60	0.01	0.062	10	27	74 mV/fF
[44]	CBCM + osc	semi-digital	180	1.8	0.10	0.01	0.07	0.0645	873	138 pulses/fF
[46]	C2I	analog	65	2.5	0.22	0.002	1.8	0.03	800	5 nA/fF
[57]	C2T	semi-digital	180	1.8	0.20	-	21	0.17	10.77	3.62 ns/fF
[58]	C2T	semi-digital	130	1	0.06	3.40	10700	0.08	1	7 ns/fF
[59]	C2T	semi-digital	350	3.3	16.5	0.05	0.4	0.2	900	-
[60]	C2T	semi-digital	320	3	0.08	0.38	0.256	0.52	800	32 ns/fF
[61]	C2T	semi-digital	160	1	0.01	6.86	8	0.05	255	-
[62]	C2D	digital	130	1.5	0.22	20	1	0.317	5.4	-
[63]	C2D	digital	180	1.4	0.08	1	3	0.2	53.20	-
[67]	C2D SD	digital	350	3.3	0.76	10.5	16	2	42	-
[69]	C2D SD	Digital	350	3.3	1.44	128	1	0.048	490	-
[70]	C2D SD	Digital	180	1	0.57	40	10.8	0.18	340	-
[72]	C2D SAR	Digital	160	2	9.2	100	3.8	0.33	2.5	-

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area occupation (lower than 0.3 mm^2). Finally, by inspection of Fig. 15 it is apparent that the only solutions achieving *FoM* lower than 100 and power consumption lower than 10 μW are [8], [70] and [72].

From the above considerations we can conclude that although there is no topology that always shows best overall performance, solutions based on C2D architecture (in particular those exploiting ΣΔ modulators) seem more suitable for resolutions lower than 100 fF with low area occupation and measuring time as well. On the other hand, for less stringent resolution requirements, the C2I architecture offers the lowest measuring time and seems most suitable for high-speed applications and low area occupation.

VIII. CONCLUSIONS

A review of the main electronic interface approaches for capacitive sensors has been carried out giving special emphasis to applications requiring sub-femtofarad resolutions. The comparison shows that adoption of a specific topology depends upon the constraints given by the particular application and that a generalization cannot be performed. Nonetheless, data-driven comparison of the state-of-the-art solutions reveals that the C2D SD approach achieves an overall good balance between resolution, speed and area occupation as provides the best figures of. The C2I approach offers the lowest measuring time and is hence most suitable for high-speed applications with lowest silicon area occupation.

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