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### CLB TEST REPORT

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### Abstract

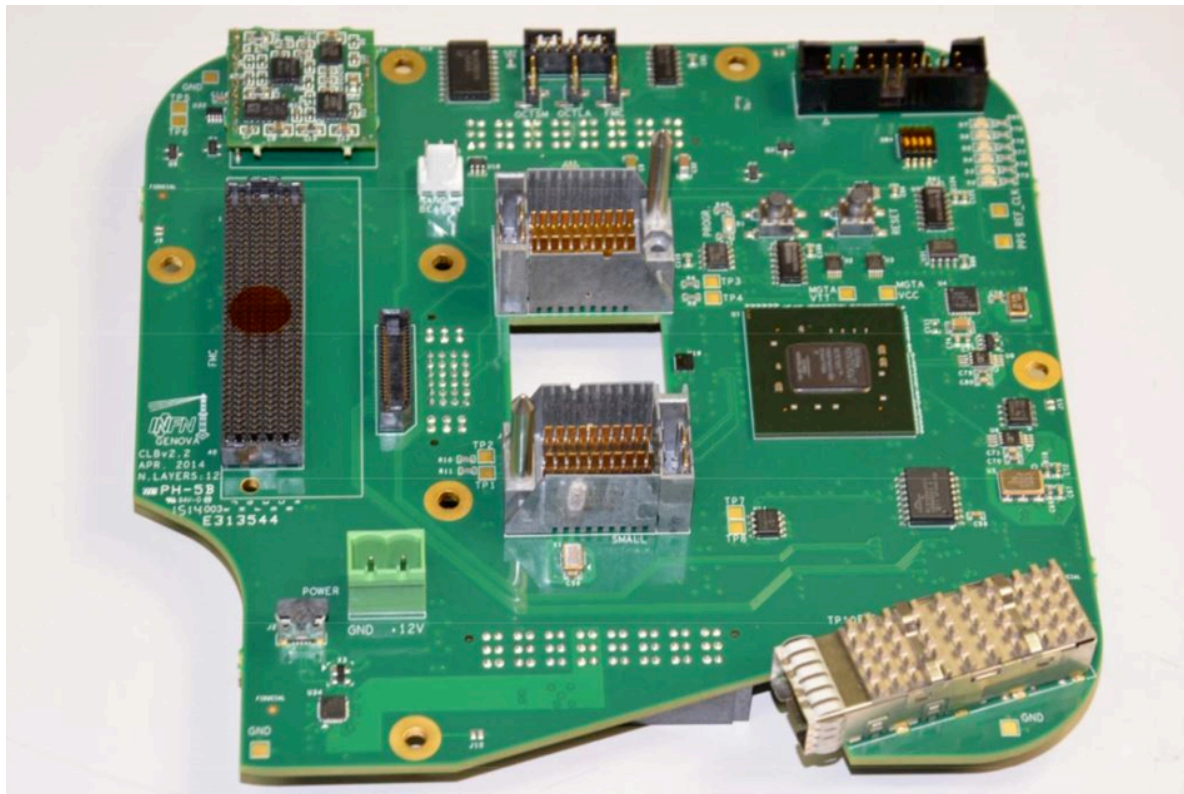
In this note we describe all tests performed on the Central Logic Board (CLB). The CLB is designed to manage slow control instrumentations and PMT data for each Digital Optical Module (DOM).

PACS:07.50.-e

## 1 INTRODUCTION

The Central Logic Board (1) is the board dedicated to acquire the data from PMT and instrumentation, pack them and send them to the on shore station through UDP packets. The CLB is located inside the DOM and its dimensions are about 150x150 millimeters.

The Central Logic Board hardware and firmware has been tested in different steps (with the production of 2 prototype batches, the first one of 6 CLBs (CLBv2.0) and the second one of 12 (CLBv2.2 ) and different places; A Picture of the CLB board version 2.2 is shown in Figure 1.



**FIG. 1:** The CLB v2.2 board. FPGA side

The present document is a report of the all performed tests.

The locations involved in the CLB tests are:

- IFIC – Valencia
- INFN – Bologna
- INFN – Genova
- NIKHEF – Amsterdam

An ELOG (2) has been used during the test and debug phase to help all the involved

people to keep track of the improvements.

In the following sections we will report the Hardware Tests perform on:

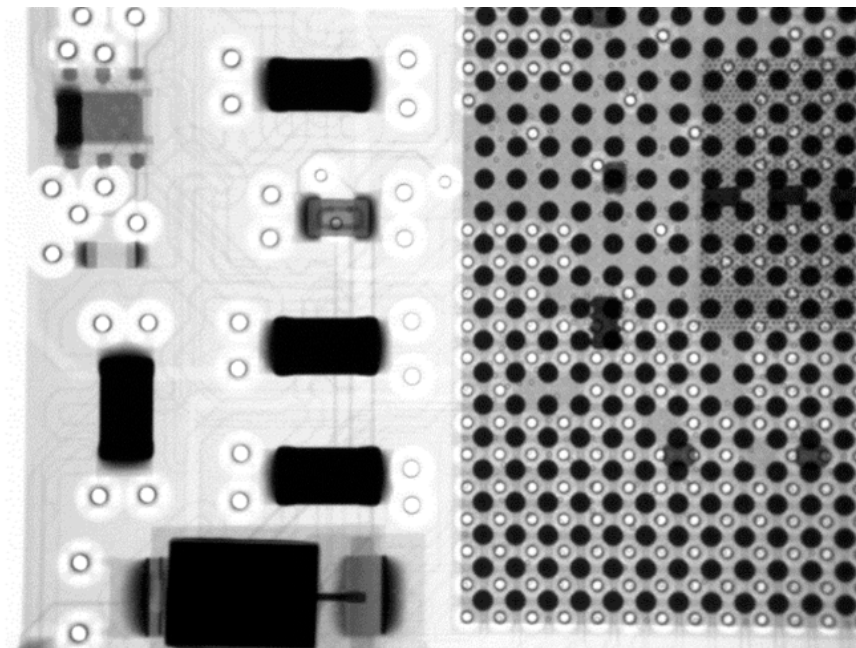
- X-Rays analysis
- JTAG Chain
- In-Rush Current
- Optical Link
- PMT Signals
- Acoustic
- Nanobeacon
- Expansion Connectors
- Thermal Analysis
- EMI analysis
- Life Test

And the Software Tests perform on:

- White Rabbit
- PMT
- Instrumentations

## **2 X-RAYS ANALYSIS**

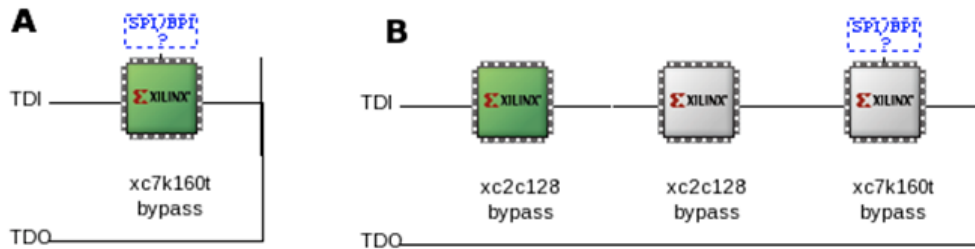
After the production of the first prototypes, an X-Rays scan was performed on the CLBs; no defects were observed. A sample of the analysis is shown in Figure 2.



**FIG. 2: X-Rays analysis of CLB: FPGA side**

### 3 JTAG CHAIN / FPGA / SPI FLASH

The JTAG chain has been tested with and without the Octopus Boards plugged on the CLB. The Xilinx Impact software installed in a PC was used to check the chain; the Boundary Scan is shown in the figure below. In Figure 3A only the CLB FPGA is present (case without Octopuses); in Figure 3B, instead, also the 2 Octopus Board CPLD are seen by the Boundary Scan.



**FIG. 3:** Figure 3: Xilinx Impact JTAG Chain. A = no Octopus; B = with Octopus

When no Octopus boards are plugged on the CLB, the J17 and J20 jumpers (3) were present on the CLB. A simple LED controller firmware has also been loaded on the S25FL512 SPI Flash Memory connected to the FPGA; after a new power up of the board, the firmware was correctly loaded in the FPGA from the memory.

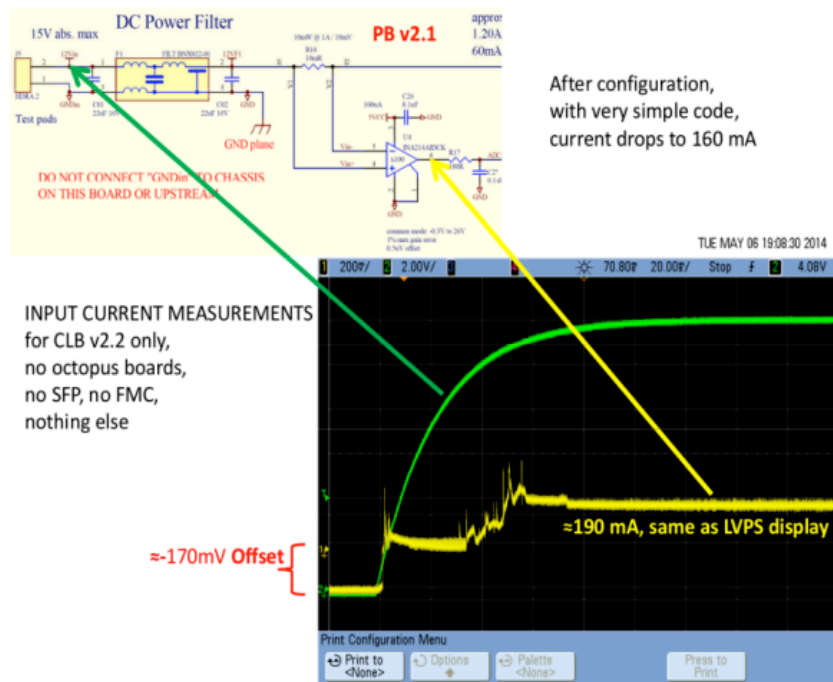
*An issue was encountered in the first prototype phase: the chosen Flash Memory (Numonix 1Gb) was not compatible with the Xilinx Impact software. It was decided to change this component to the current one (Spansion 512 Mb ) to solve the problem.*

### 4 IN RUSH CURRENT

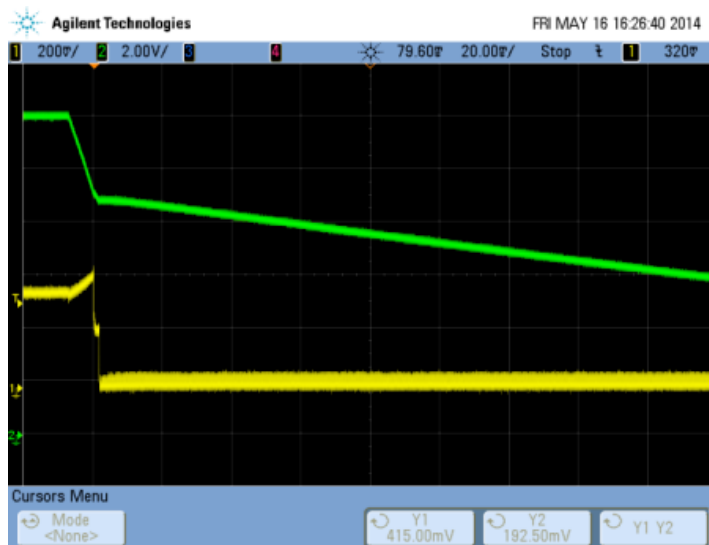
Several measurements of the in-rush current were done. The results show that there is no dependence from the loaded firmware; the only difference consists in the absorbed current needed by the firmware at the end of the download.

In-Rush current measurement, by monitoring the current from the Power Board with a simple LED controller firmware loaded from the Flash Memory is showed in Figure 4; No critical peaks of current were found .

A current analysis during the power off was also performed, showing a little peak of current (see Figure 5).



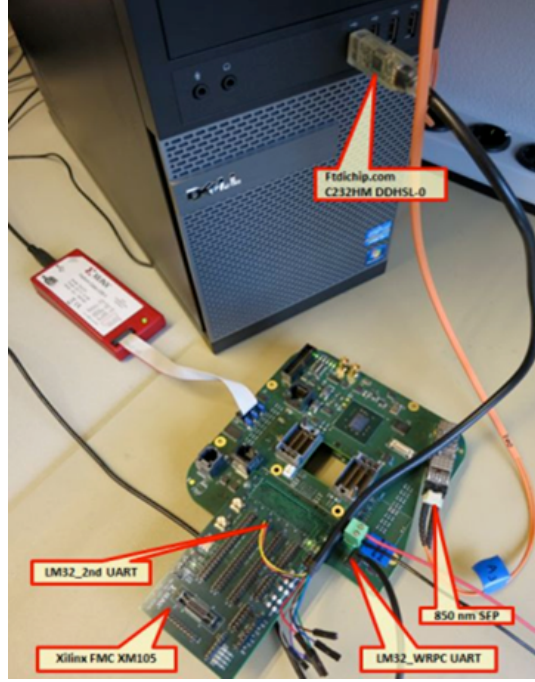
**FIG. 4:** In-Rush current measurement



**FIG. 5:** Current measurement at power off; a little peak of about 65 mA was measured

## 5 OPTICAL LINK

The first optical link test was performed by connecting the CLB to an optical network card installed on a Linux machine; an UDP packet was sent from the CLB to the PC and vice-versa using the setup shown in Figure 6.



**FIG. 6:** Optical link test setup

Other optical communication tests followed this one, in order to test also the firmware functionality.

## 6 PMT SIGNALS

### Preliminar test

A first simple test on the PMT signal was performed by using a Pseudo Octopus board and a Digital Pattern Generator (see Figure 7).

The Pseudo Octopus board was sequentially plugged in the Octopus Large and Small connector, while the Digital Pattern Generator was sending a slow signal (rate about 0.5 s) to set/unset all of the PMTs. A simple firmware was used to check the input on the corresponding pins and show the result on a shell connected to the PC via USB.

All PMT signals changed as expected. The oscillators switch on/off has been tested, too; the 10 MHz clock was monitored with the oscilloscope; it is ok.



**FIG. 7:** Pseudo Octopus board plugged on a CLB

### **PMT test**

A dedicated setup is used to test the capability to operate and read out a (part of a) DOM. In this setup a power board v2.1 is used attached to a CLB v2.2. Via a USB connection between the CLB and a PC a connection can be established via a terminal with the LM32 running on the FPGA. This is used for operation and monitoring purposes. The operation includes the slow control commands for performing the state transitions, setting initialization and configuration parameters, and starting and stopping runs. The initialization and configuration values can also be monitored via this link, as well as the status of each of the 31 PMT channels.

The fiber from the CLB is connected to an optical network card in the PC. Once PMT channels are enabled, and the system is in state running, data are sent in UDP packets by the CLB to the PC via this link.

The setup is equipped with a pseudo octopus board connected to the small octopus connector, and an octopus large board v3 connected to the large octopus connector. The pseudo octopus board is connected to a pulse generator, and 8 PMT modules (each with a Ham\_Promis2\_v1 PMT base) are attached to the large octopus board.

As a first test the high voltage was left off and no input was generated by the pulse



generator. It was verified that when PMT channels are enabled, and the system is in state running, UDP packets arrive on the PC side. These packets are empty frames, only containing the common CLB header with a size of 28 B. The data format of this header in the UDP packets is as specified. The frequency of the packets (10 Hz) is in accordance with the setting of the frame duration (default 100 ms). The frame duration is configurable. It was verified that when the frame duration is changed, the packet frequency changes accordingly.

The values of the fields in the CLB header have been verified, as far as implemented: the frame index is as expected, the value of the timestamp field is in accordance with the setting of the frame duration, and the MAC address was found to correspond to that of the CLB.

As a next step the pulse generator was switched on and the channels on the pseudo octopus board were enabled. When the system is in state running the signals from the enabled channels are added to the payload of the UDP packets. The data of a pulse are stored in a PMT item with a size of 6 B. The PMT items are appended to the CLB header. When the number of PMT items exceeds the maximum number of PMT items that can be stored in a UDP packet, a new packet is generated (starting with the CLB header) and sent. It was verified that a new packet is generated when the maximum packet size is reached, and that the frame index is incremented for these packets accordingly. The maximum packet size is configurable (default 8972 B). It was verified that when the setting of the maximum packet size is changed, the actual packet size changes accordingly.

The format of the PMT items in the UDP packets is as specified. The values of the fields in the PMT items have been verified: PMT items carry the ID of the enabled channels and the pulse width is in accordance with the setting of the pulse generator. The number of PMT items in a packet corresponds to the pulse frequency of the pulse generator. Changing the pulse frequency and pulse width of the pulse generator changes the packet size and the pulse width in the PMT items accordingly.

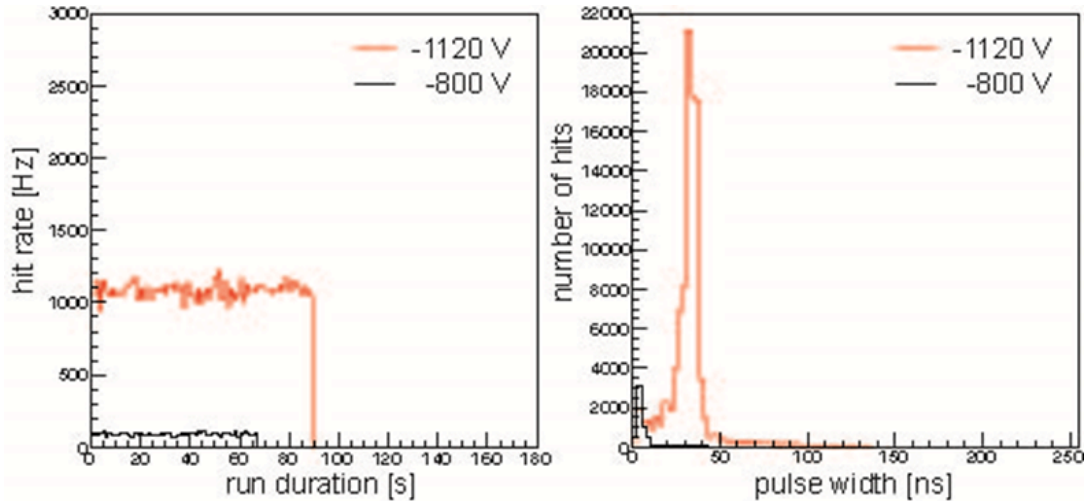
To check whether the voltage is correctly set to the PMT base with the prescribed slow control commands, an empty PMT base (without PMT) was connected to the large octopus board. By giving the appropriate slow control commands for switching on the high voltage, enabling this channel (leaving all others disabled) and initializing and configuring the system, it was verified with a multimeter that the high voltage is actually and correctly set to the PMT base.

When complete PMT modules are enabled, the setup is put in the dark. The status of all PMT channels can be monitored with a slow control command. When the high voltage is switched on, and the 8 channels with a complete PMT module are enabled, and the system is configured, it was verified that the PMT bases are correctly detected with their corresponding ID and that the enabled/disabled setting is correctly displayed for each channel. The high voltage and threshold are also shown for each channel (default -800 V and 1069 mV respectively).

When a run is started, it is verified that the UDP packets contain PMT items from all 8 enabled channels. Looking at the timestamps of the subsequent UDP packets it was verified



that there was no packet loss for a run lasting for about 3 hours. The high voltage of a channel can be changed with a slow control command. Increasing the high voltage results, as expected, in a higher count rate and larger pulse widths, as can be seen in the figure below for one channel. The left plot in Figure 8 shows the hit rate (in Hz) for the default high voltage setting (black line) and for the high voltage setting as recommended by Hamamatsu (red line). The right plot shows the change in the pulse width (in ns) for the two high voltage settings.



**FIG. 8:** Hit rate in Hz (left). Pulse width in ns (right)

## 7 ACOUSTIC (PIEZO)

The acoustic instrument (Piezo) is connected to the CLB by the Octopus Large board. A switch is present on the CLB to power on/off the instrumentation; tests were made to check the proper working of the acoustic interface, by using a Piezo prototype, connected to an Octopus Large board with a piggy-back board.

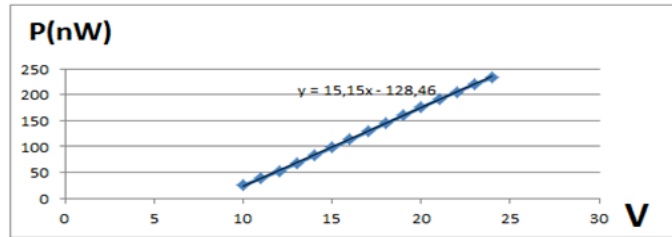
See section 17 for further details.

## 8 NANOBEACON

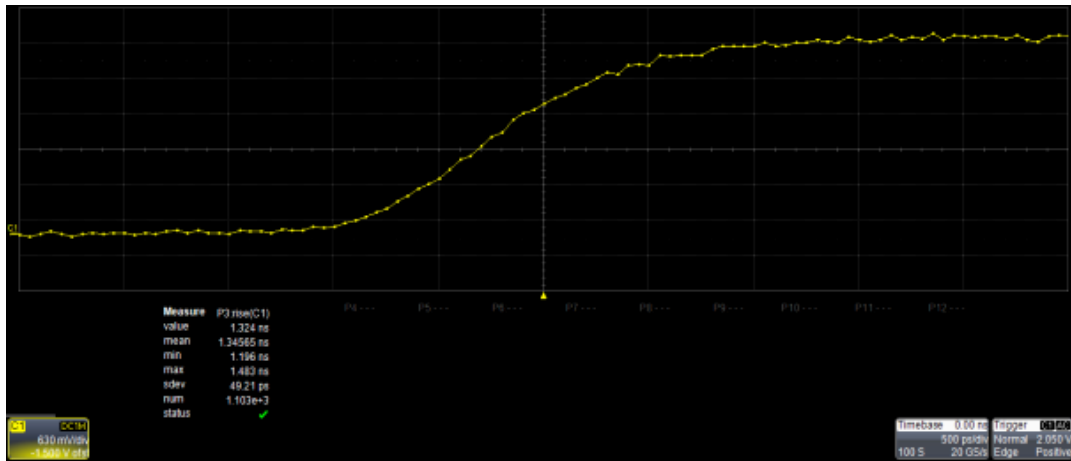
The connection between Nanobeacon and CLB is by means of connector J22. This connector provides the trigger and voltage signals to flash the LED. Optical power tests have been performed, flashing the LED with different voltages as shown in Figure 9.

The nanobeacon trigger rise time was also tested. More than 1100 pulses have been measured. The mean of the rise time (10%-90% interval) was 1.34 ns with an standard deviation equal to 49 ps as shown in Figure 10.

Nanobeacon board 14014120011	
LED_Voltage(V)	E(nW)
24	233,36
23	220,13
22	205,74
21	190,99
20	175,46
19	159,92
18	144,49
17	128,85
16	113,1
15	98,13
14	82,85
13	67,45
12	52,56
11	38,49
10	24,89



**FIG. 9:** Optical power test



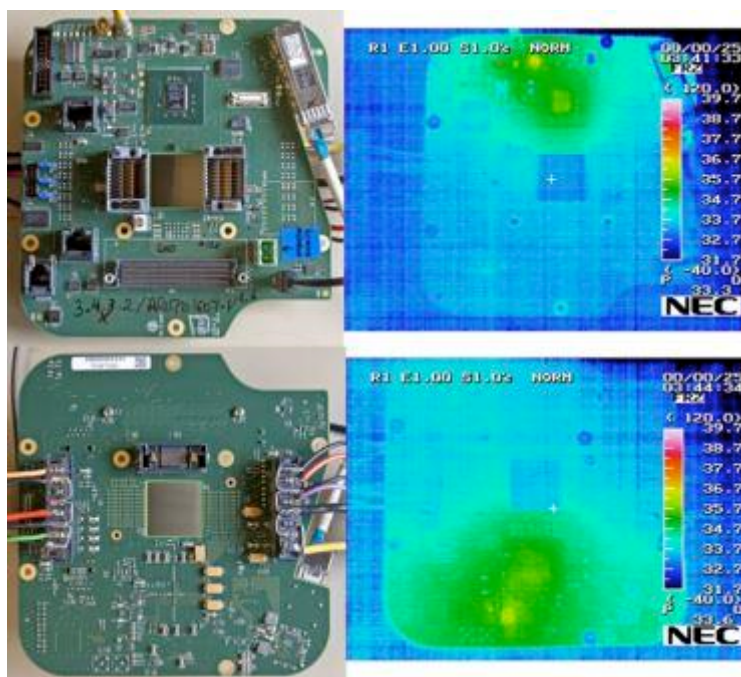
**FIG. 10:** Nanobeacon trigger rise time

## 9 EXPANSION CONNECTORS

Simple loop-back tests have been performed on the J32 20 pin Header connector and J34 FMC connector (3), mainly to check the correctness of the firmware User Constraint File.

## 10 THERMAL ANALYSIS

A thermal analysis has been performed on the first CLB prototypes (see Figure 11). The CLB was running a firmware with White Rabbit PTP in Track\_Phase. The ambient temperature was around 23 °C; the FPGA and the SFP Laser were around 36 °C, while the Clock driver (U4) was around 37 °C.

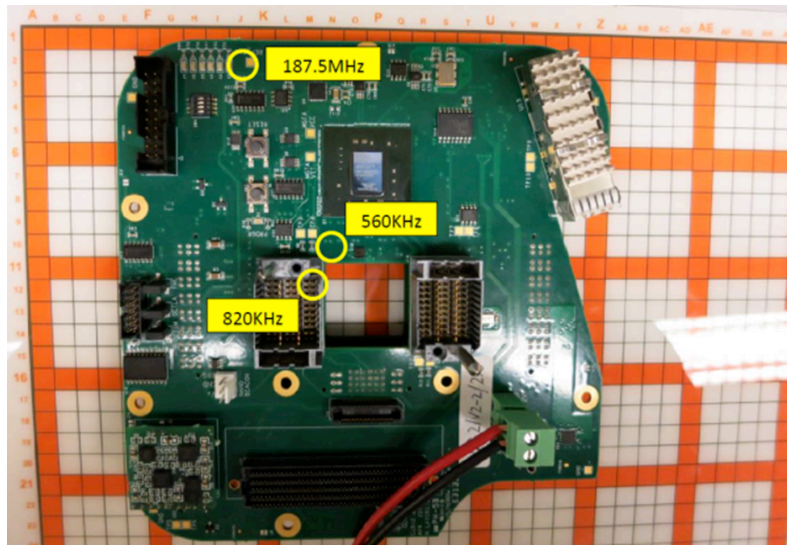


**FIG. 11:** Thermal analysis: CLB top (upper left) with thermal picture (upper right); CLB bottom (bottom left) with thermal picture (bottom right).

## 11 EMI ANALYSIS

3 hot spot has been found at frequencies 560, 820 KHz and 187.5 MHz (see Figure 12). The first two are due to DC/DC converters: A plate between the CLB and the PB will minimize the induced noise. The one at 187.5 KHz is due to the test clock signal. This signal will not be present at final operation.

An extensive report on EMC has been prepared, see (4).



**FIG. 12:** EMI hot spots found on the CLBv2.2.

## 12 HIGH ACCELERATED LIFE TEST

In a climatic chamber a CLBv2.2 + PBv2.2 has been switched on (see Figure 13). The FPGA ran the last version of the firmware. Only the 12 V were connected (Not Octopus, no SPF, etc). The test started at 60°C, after two hours the CLB communications (SFP) and Nanobeacon were tested and the temperature was increased 5°C. The boards worked fine up to the limit of the climate chamber, 150°C.



**FIG. 13:** CLBv2.2 inside the climatic chamber for the HALT test.

As the temperature increased the current consumption increased. When the temperature was increased to 120 °C the current consumption arrived to 1 A and then it disconnected. (probably due to a DC/DC safety disconnection). The result of this test can be considered very satisfactory for both the CLB and the PB.

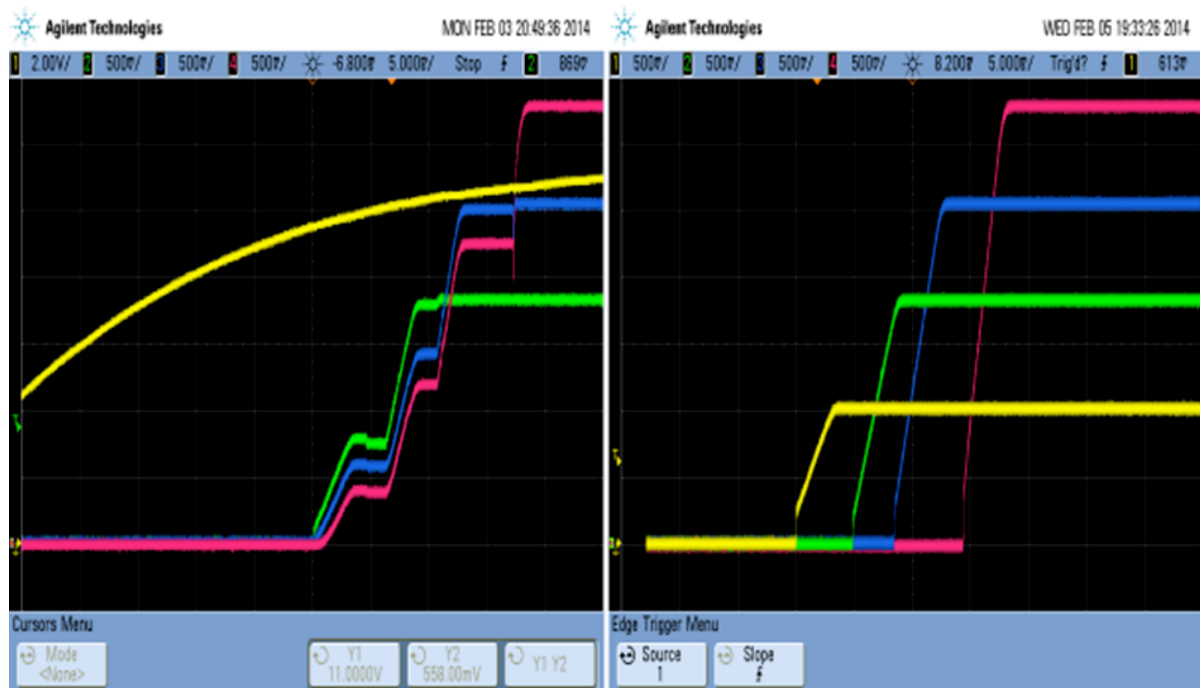
### 13 PROBLEMS DETECTED

During the test phase of the first prototype batch, 2 CLB and 2 PB broke up. After more deep tests, the problem was found in the used power supply, which showed a very slow rising ramp. This, combined with the PB, generated several restarts on the needed power rails each start up, which lead to the FPGA breaking and the consecutive damage to the rest of the both CLB and PB boards (see Figure 14)



**FIG. 14:** Start up measurements on 1.8V (green), 2.5V (blue), 3.3V (red) and 12V (yellow), by using the "slow" power generator; several restarts were caused, which lead to the FPGA breaking.

In addition the ramp-up of the PB rails was found to be not in respect with the Xilinx specifications; the presence of inter-rails diodes caused a bad shape on the rising voltages, which could have contribute in the FPGA breaking (see Figure 15).



**FIG. 15:** Ramp up measurements of the 1 V, 1.8 V, 2.5 V, 3.3 V from the Power Board; on the left the results when inter-rails diode were present on PB, on the right the result when no inter-rails diodes are present.

A different power supply was used from this point on, but several other tests were performed, in particular on the power board to improve the ramp up. In addition the CLB was powered for a while with external power supplies, without the PB; the following currents were measured:

Rail	Current (no firmware)	Current (with firmware, not complete)
1.0 V	73 mA	213 mA
1.8 V	75 mA	107 mA
2.5 V	3 mA	3 mA
3.3 V	330 mA	269 mA

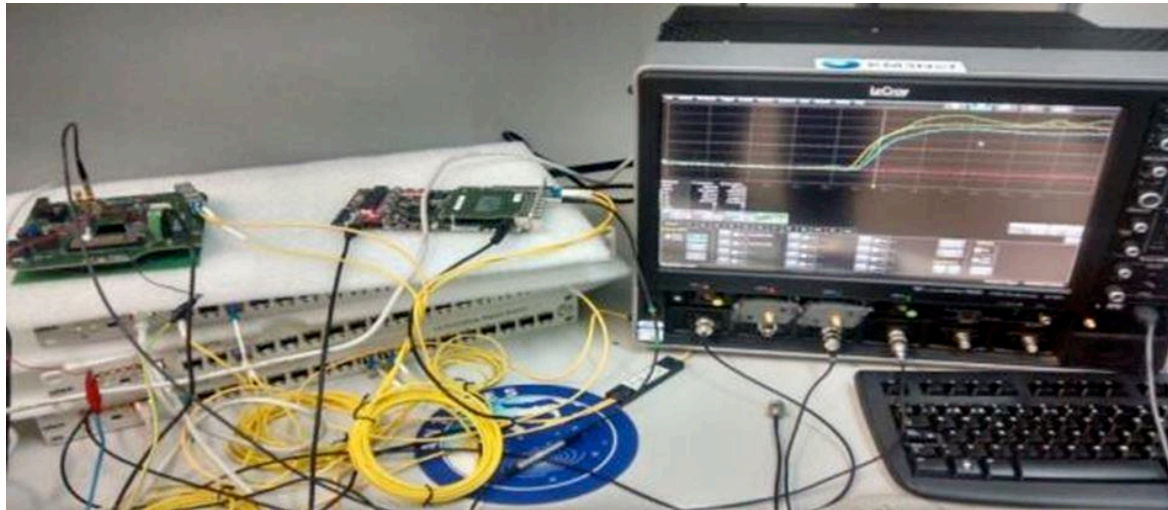
*The 2 broken CLB were repaired, by substituting the FPGA, the Clock Generator U4. In one board also the broken Temperature and the Tilt & Compass sensors were removed.*



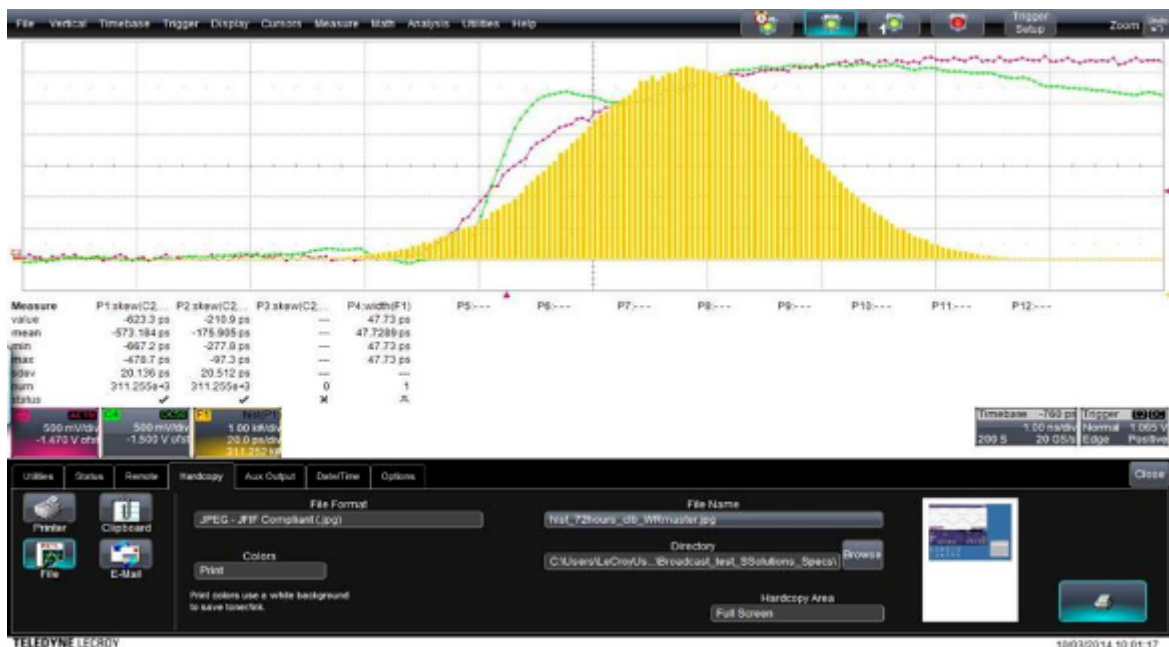
## 14 WHITE RABBIT TIME SYNCHRONIZATION

White Rabbit Time Synchronization has been tested by using the On-shore Station prototype. Figure 16 shows the test bench with one CLB and one SPEC board (The SPEC board is the White Rabbit evaluation board) connected to the On-Shore Station prototype.

The synchronization of the CLB with respect to the WR master switch is tested. Figure 17 shows the skew between the PPS signals of both devices (47 ps of standard deviation).



**FIG. 16:** White Rabbit On-shore station test setup.

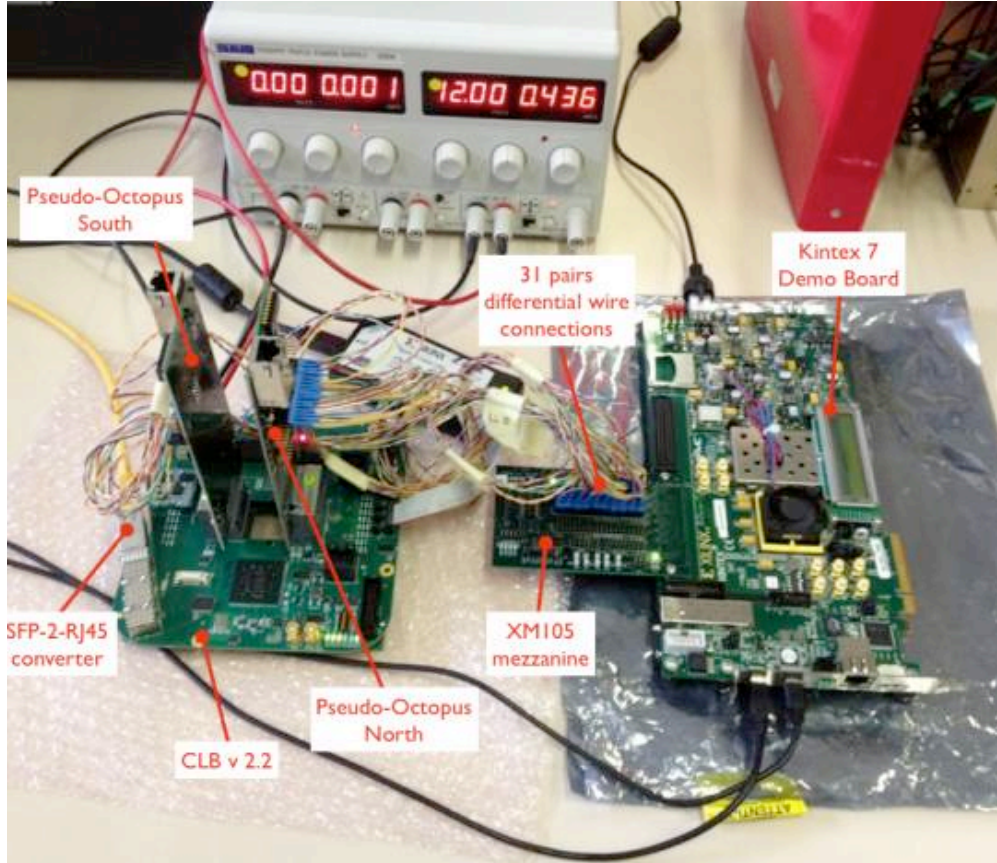


**FIG. 17:** White Rabbit synchronization results.



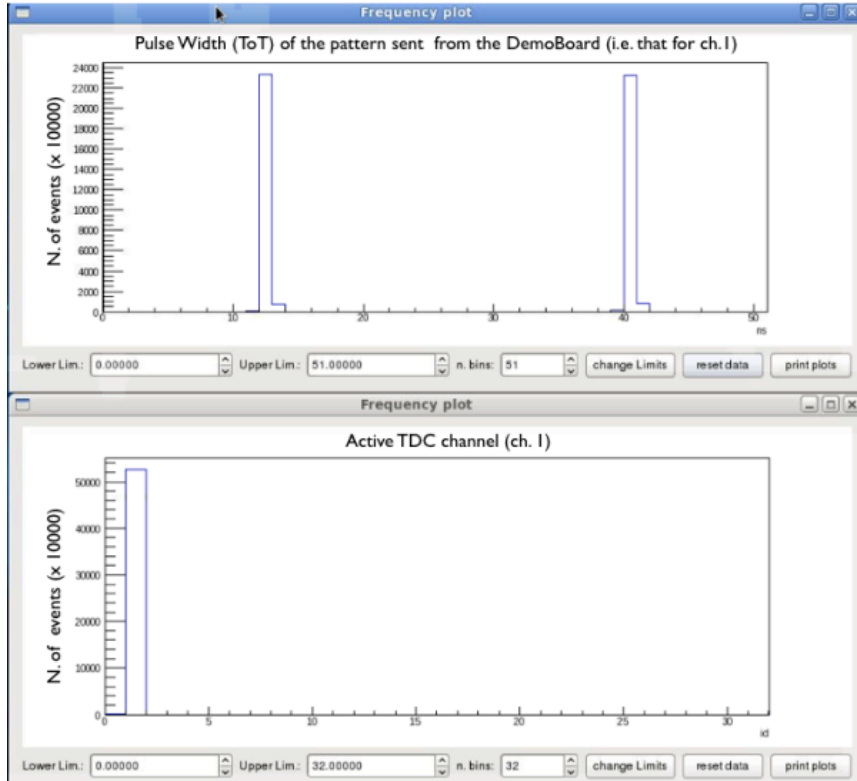
## 15 TDC

Time to Digital Converters (TDC) readout system is sampling the LVDS signals coming from PMTs. PMTs are connected to CLB through Octopus boards. Several tests were made to check the proper TDC readout behavior by using a PMT simulator implemented on FPGA and connected to CLB by pseudo-octopus board as shown in Figure 18.



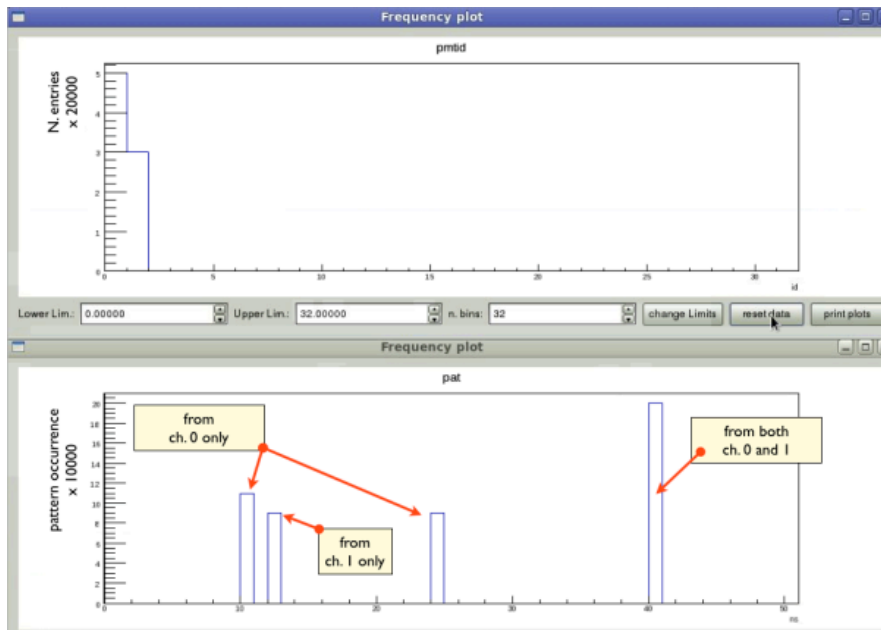
**FIG. 18:** TDC test setup.

Different patterns are sent from the PMT simulator to the CLB by using pseudo-octopus board. The TDC data are sent from CLB to computer via optical link and analyzed using a software interface developed in Bologna. The results in one channel, with 1 ns of resolution, for two trains of pulses of 12 ns and 40 ns with a 5 KHz rate are shown in Figure 19.



**FIG. 19:** TDC results for pulse width of 12 ns and 40 ns.

Other tests were performed with two channels active. Two patterns were generated with different number of pulses (Ch0: 24-40-10 ns; Ch1: 12-40 ns), for this reason the entries of the bin @ 40 ns is twice larger than others. The results for this test are shown in Figure 20.

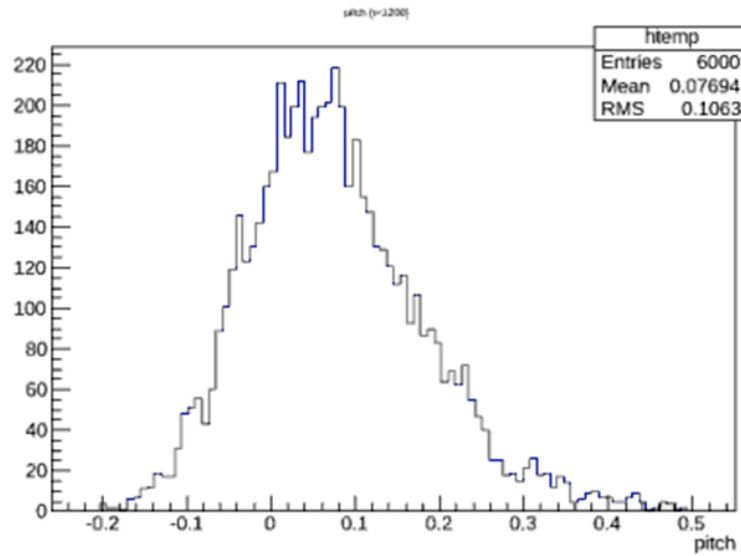


**FIG. 20:** TDC results for two channel active (Ch0: 24-40-10 ns; Ch1: 12-40 ns).

## 16 TEMPERATURE, TILT & COMPASS

The temperature and tilt & compass sensors are connected to the CLB's FPGA using an I2C bus. The communication with these devices has been tested by reading some data and displaying the results on the shell (USB debug communication with the CLB).

Additional tests have been performed on the tilt & compass; the stability of pitch and roll was found to be better than  $0.1^\circ$  (see Figure 21), while for the yaw, the strong influence on the magnetic field of the external power supply used, lead to stability worse than  $1^\circ$ .

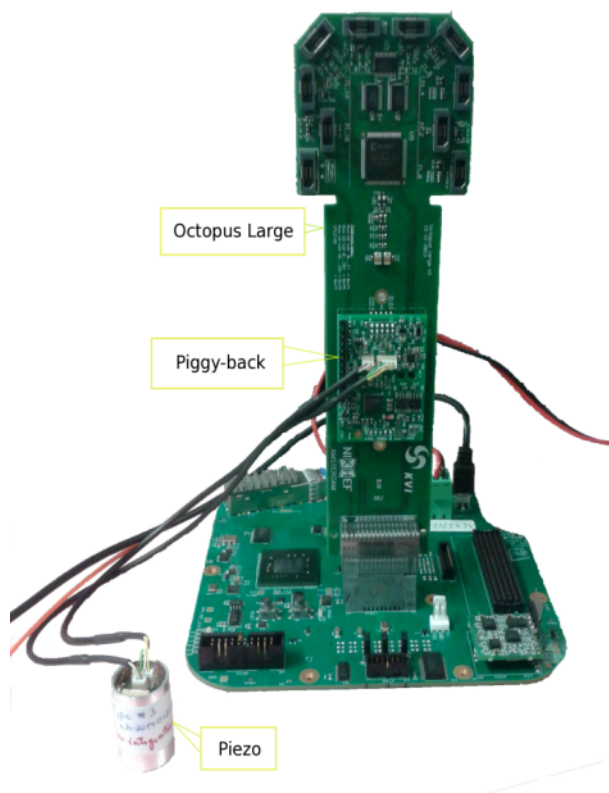


**FIG. 21:** Tilt & Compass test: pitch stability.

Detailed tests on the Tilt & Compass are reported in (5).

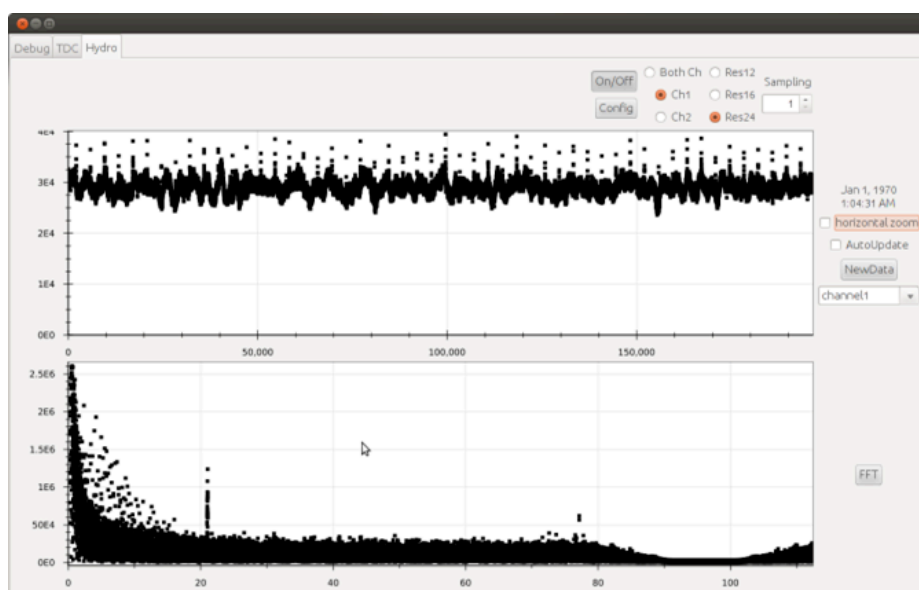
## 17 ACOUSTIC (PIEZO)

Several tests have been performed on the acoustic interface; for the first prototype batch, a hydrophone prototype connected to the CLB with the dedicated RJ45 connector was used. Later the acoustic interface was changed, by leaving only the Piezo interface, with LVDS signals through the Octopus Large board; the used setup for the test is shown in Figure 22.



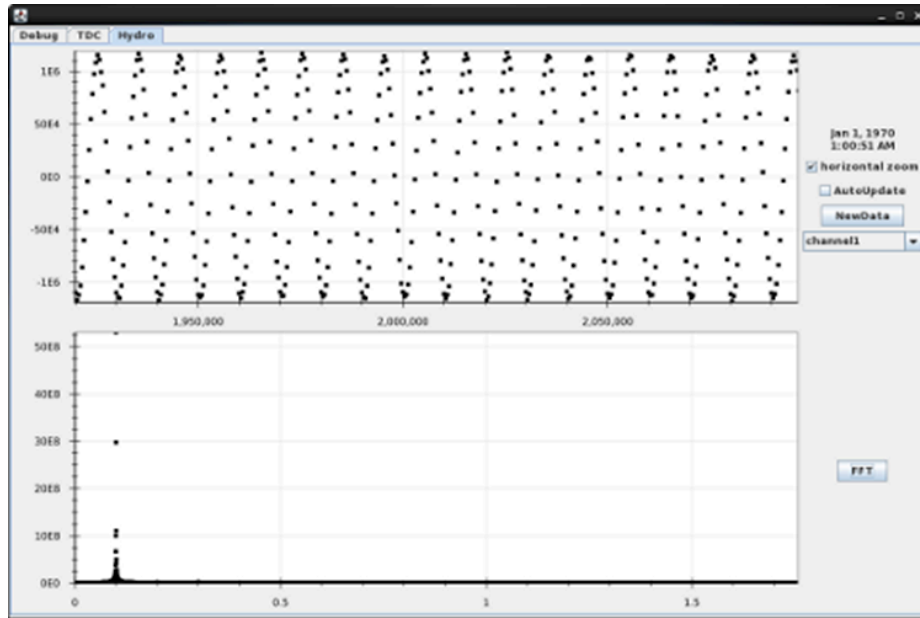
**FIG. 22:** The Piezo is connected to CLB through a piggy-back board on the Octopus Large.

The acoustic module in the firmware have been tested by sending the data in UDP packets (as they will be sent after the deployment) via copper Ethernet, using a debug FMC board. Data were then acquired and analyzed by a dedicated Java software (see Figure 23).



**FIG. 23:** Acoustic data acquired from the Piezo (top), with FFT analysis (bottom).

The tests performed with the first CLB prototypes and the hydrophone prototype, which had the possibility to use a waveform generator as input signal, showed that the data are correctly acquired and decoded, without losses (see Figure 24).



**FIG. 24:** Acoustic data acquired from the hydrophone prototype, using a sinusoid with 100 Hz of frequency. The real time audio signal (top) and its FFT (bottom) are visible.

## 6 REFERENCES

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