High performance n^+/p and p^+/n germanium diodes at low-temperature activation annealing

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ARTICLE INFO

Article history:

Received 16 July 2010

Received in revised form 5 October 2010

Accepted 11 November 2010

Available online 16 November 2010

Keywords:

Germanium

Junction diodes

Low temperature phosphorus activation

Platinum germanide

ABSTRACT

In this work we demonstrate the fabrication and characterization of high performance junction diodes using annealing temperatures within the temperature range of 300–350 °C. The low temperature dopant activation was assisted by a 50 nm platinum layer which transforms into platinum germanide during annealing. The fabricated diodes exhibited high forward currents, in excess of 400 A/cm² at $\sim|0.7|$ V for both p^+/n and n^+/p diodes, with forward to reverse ratio I_F/I_R greater than 10⁴. Best results for the n^+/p junctions were obtained at the lower annealing temperature of 300 °C. These characteristics compare favorably with the results of either conventional or with Ni or Co assisted dopant activation annealing. The low-temperature annealing in combination with the high forward currents at low bias makes this method suitable for high performance/low operating power applications, utilizing thus high mobility germanium substrates.

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1. Introduction

Germanium is being considered as an alternative semiconductor material for CMOS logic applications, due to the performance limitations of the scaled silicon based devices [1–3]. The main advantage of germanium as a channel material is the high electron and hole mobility which could result in performance enhancement of the Ge based devices in comparison to the Si ones [4]. Towards this direction, significant progress has been accomplished, since p-channel-metal oxide semiconductor field effect transistors (MOSFETs) have already been fabricated either on germanium or germanium on insulator substrates with an effective channel length of ~ 70 nm that showed the validity of the overall approach [5,6]. However, the fabrication of n-channel MOSFETs is quite challenging mainly due to surface passivation issues, which are more intense for the case of n-channel [7–9] and also by the requirement to fabricate shallow low sheet and contact resistance n^+/p junction diodes for the source and drain regions [10]. As in the case of silicon, germanium surface passivation is one of the key technological issues which must be addressed in order to implement proper MOSFET operation [7]. The thermodynamic and kinetic control of the Ge/GeO₂ [11] interface allowed recently the demonstration of large channel length n-MOSFET with record-high electron channel

mobility, a development that relaxes the constraints of the interfacial passivation issue [12]. Another problem of the n^+/p diode fabrication is impeded by the behavior of the donor dopants which have a low solid solubility limit in germanium that combined with the concentration enhanced diffusion effect results to fast in and out diffusion towards the bulk or towards the surface, reducing thus the dopant concentration in the near-surface region [13].

Boron incorporation into n-type Ge via ion implantation is rather straightforward. The implanted boron ions show two prominent characteristics. They exhibit limited diffusion even after high temperature or long time annealing [14] and they occupy substitutional lattice sites even without a post-implantation annealing [15]. The majority of the ion-implantation induced defects can be annihilated by a low-temperature annealing below 400 °C [15]. At high implantation doses, the formation of stable B-related clusters seems as the most probable reason that inhibits the full activation of the boron implants [13–16]. This can be surpassed by the technique of pre-amorphization implant where the solid state regrowth of the amorphous near-surface region results in high boron activation, being of the order of 2.4×10^{20} cm⁻³ [14].

Since n-type dopants such as P and As are heavier ions than boron their introduction into Ge lattice results in significantly higher damage in comparison to that produced by boron implants [17]. The ion-implantation induced defects are considered to be vacancy-dopant clusters, forming mostly acceptor type centers, which constitute a considerable carrier removal source [18]. The

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implanted region exhibits a p-type conductivity [19]. The restoration of the lattice disorder requires a higher post-implant thermal budget, with annealing temperatures higher than 500 °C [13,20]. However, experiments showed that regardless of the annealing scheme (furnace annealing [21], rapid thermal annealing [13], laser annealing [22], or flash lamp annealing [23]) the final result, in most cases is the so-called box-like dopant concentration depth profile driven by the concentration enhanced diffusion [24]. This behavior constitutes a significant obstacle to the formation of shallow n⁺/p junctions, which are required for state of the art field effect devices. A recent report indicates that millisecond flash lamp annealing in preamorphized Ge substrates implanted with P, showed negligible phosphorus redistribution with an activation level of $6.5 \times 10^{19} \text{ cm}^{-3}$ [25].

The above reports indicate that the issue of dopant activation via a post-implantation thermal treatment faces significant obstacles and therefore other approaches are urgently required. Dopant activation under the influence of a metal layer (cobalt or nickel) in direct contact with an implanted germanium region has been recently employed for the formation of shallow n⁺/p and p⁺/n junction diodes using low thermal budgets with typical annealing temperatures lower than 380 °C [26,27]. This method constitutes an alternative approach for dopant activation, since it is based on the solid state reactions of the metallic element with the Ge substrate atoms [28] and the accompanied side effects of these reactions. These include the dopant redistribution due to the formation of metal germanide alloy (the so-called snow-plough effect) [29], the metal induced crystallization [30,31] and the metal induced dopant activation effects [32]. In this work we report the fabrication, the structural and the electrical characteristics of n⁺/p and p⁺/n germanium junction diodes assisted by a platinum layer using low annealing temperatures within the range of 300–350 °C.

2. Experimental

The formation of the fabricated Ge diodes is based on a single mask layout and the fabrication sequence is shown schematically in Fig. 1. Initially, n- and p-type (100) germanium substrates with resistivity of 1–2 Ω cm were firstly degreased by acetone and propanol and subsequently by a 2% HF solution. After cleaning, a 100 nm SiO_x layer was deposited by sputtering at room temperature. This layer serves as a hard mask and partially as a passivation

Fig. 1. Schematic diagram which shows the major processing steps and the fabrication sequence of the fabricated germanium diodes used in this work.

layer. In order to accomplish controllable etch rates, an annealing step was performed at 450 °C for 30 min in an O₂ ambient for the densification of the SiO_x layer. Photolithography was then used to define the active diode area, consisted of squares patterns with areas $300 \times 300 \mu\text{m}^2$, $100 \times 100 \mu\text{m}^2$ and $50 \times 50 \mu\text{m}^2$, followed by a buffered oxide etch (BOE) step for 1 min. Without removing the photoresist, the n-type samples were ion implanted using 50 keV BF₂ ions of $2 \times 10^{15} \text{ ions/cm}^2$ dose, while the p-type samples with 25 keV P ions of $2 \times 10^{15} \text{ ions/cm}^2$ dose. The photoresist therefore acts as an additional implant stop layer. The ion beam was tilted by 7° with respect to the normal of the sample surface to minimize channeling and the beam current was kept low at 2–3 μA to avoid excessive heating of the remaining photoresist. The projected range of the implanted boron ions was 35 and 27 nm for the phosphorus ions, as estimated from the SRIM code. After ion implantation the samples were degreased by dipping in BOE for 30 s, followed by deposition of a 50 nm platinum layer. A lift-off step was then applied which removes the photoresist and the platinum layer except from the active diode regions. Annealing of both dopants was performed at a temperature of 350 °C for time intervals ranging from 2 to 30 min using a furnace in N₂ ambient. A second split of samples was also prepared where lower annealing temperatures of 300 °C were tested.

Control diode samples with Pt deposition and without annealing were used to monitor the initial conditions of the junction diodes. The ohmic back contact of all samples was made by In–Ga eutectic alloy. The experimental methodology that was followed in this work consisted of the following steps:

- Study of the thermally induced solid state reactions between the Pt layer and the Ge substrate which leads to the formation of the platinum germanide layer and was carried out by X-ray diffraction (XRD) measurements at room temperature. The formation of the platinum germanide was conducted in both un-implanted and implanted germanium substrates. In the case of the un-implanted Ge substrates, 50 nm of platinum was deposited at room temperature on (100) Ge substrates. The Pt/Ge structures were then annealed in a furnace in N₂ ambient using either an isochronal or an isothermal scheme. The samples were thus annealed either for 30 min within the temperature range of 300–450 °C (isochronal annealing), or at 350 °C for time intervals between 2 and 30 min (isothermal annealing).
- Study of the dopant redistribution during the formation of the Ge_xPt_y layer. Since the Pt layer resides on top of the implanted region and the formation of the Ge_xPt_y layer consumes Ge, the implanted dopant atoms will be affected by the germanidation process. The chemical profiles of the implanted species, as well as, the Ge and Pt depth profiles were determined using secondary ion mass spectrometry (SIMS).
- Evaluation of the electrical measurements of the diodes was performed at room temperature and in the dark. The current–voltage (I–V) characteristics were measured by a HP 4140B picoammeter while the capacitance–voltage (C–V) characteristics by using a HP 4084A LCR meter.

3. Results

3.1. XRD results

The XRD spectra of the non-implanted samples after the isochronal annealing are presented in Fig. 2a. The XRD spectra are presented within the 2θ range of 20–51° for clarity. No reaction takes place in the as-deposited case since all peaks arise from Pt reflections. After annealing several XRD peaks are evident, corre-

Fig. 2. XRD spectra of the germanidation process after annealing of an unimplanted Ge substrate with a deposited 50 nm layer of Pt. (a) Isochronal annealing for 30 min within the temperature range 300–450 °C. Line A corresponds to the as-deposited state, while line B corresponds to 300 °C anneal, line C at 350 °C, line D at 400 °C and line E at 450 °C. (b) Isothermal annealing at the temperature 350 °C for time intervals 5 to 30 min. Line F corresponds to 5 min anneal, line G to 10 min, line H to 20 min and line C (which is the same to that of Fig. 2a) to 30 min.

sponding to the formation of different Pt_xGe_y phases which are listed in Table 1. In each annealing temperature different platinum germanide phases coexist with comparable intensities. For example, at the lowest annealing temperature of 300 °C (Fig. 2a-curve B) the Ge-rich phase (Ge_2Pt -B4) and the Pt-rich phase (Ge_3Pt_2 -B6) appear. However, after annealing at 450 °C (Fig. 2a-curve E) the main diffraction peaks arise from GePt (D1), Ge_2Pt (C4), and $GePt_2$ (D5) which indicates the increase of the Ge-rich phases [28]. As will be shown in SIMS measurements the formation of the platinum germanide results from the Ge substrate atoms diffusing into the Pt layer and from the Pt diffusion into the Ge substrate. We believe that the Pt-rich phases will originate mainly from the upper part of the structure as a result of Ge diffusion into the Pt layer. Similarly, the Ge-rich phases are formed at the lower one as Pt atoms diffuse into the Ge substrate, at least for short annealing times and low temperatures which were used in this study. The evolution of the XRD spectra with annealing tempera-

ture indicates also that an almost identical condition occurs after annealing at 350 and 400 °C deviating at the higher temperature of 450 °C. The XRD spectra of the isothermal annealing case are presented in Fig. 2b. After 5 min annealing at 350 °C no Pt phases exist, since all XRD peaks are attributed to Pt_xGe_y phases. The intensity of the peaks suggests that the reaction occurs earlier in time. Note also that the shortest annealing interval of 5 min (Fig. 2b-curve F) at 350 °C produces identical XRD spectra to the one with longer annealing at the lower temperature of 300 °C (Fig. 2a-curve B). As the time increases the XRD spectra transform gradually towards the 350 °C 30 min condition (Fig. 2b-curve C). Therefore the results of the Pt–Ge solid state reaction of un-implanted Ge substrates suggest that an annealing temperature within the range of 300–350 °C will lead easily to platinum germanide formation. In addition, during this low temperature and short time annealing several Ge_xPt_y phases coexist [28].

Fig. 3a shows the resulting XRD spectra of the phosphorus implanted samples annealed for 2 and 20 min at the temperature of 350 °C. The significantly lower signal in this case arises from the sample geometry where the diode regions occupy a fraction of the total sample area. It is evident that an annealing time of 2 min leads clearly to the formation of $GePt_3$ and Ge_3Pt_2 phases. Longer time annealing at 350 °C leads to the increase of the platinum germanide layer, as the intensity of the diffraction peaks indicates. However, in the case of the boron implanted samples the main diffraction peaks seems to arise from Pt phase reflections either in the case of the 2 or 20 min annealing times. The absence of platinum germanide reflections peaks indicates a limited reactivity between the Ge and the Pt. Thus, the above results suggest that the rate of the solid state reaction between the Pt and the Ge layer is modified by the presence of the implanted boron ions. The observed differences cannot be explained by the higher lattice disorder of the phosphorus implanted structures, since in the case of the un-implanted samples the Pt–Ge reaction occurs readily. Perhaps, this could be attributed to the presence of boron-related clusters which are stable upon low-temperature annealing. These clusters may slow-down the diffusion and intermixing which are required for the formation of the platinum germanide layer.

3.2. SIMS results

The evolution of chemical concentration profile of the implants into the Ge, together with the Pt and Ge depth distributions of the structures, for different annealing times are presented in Figs. 4 and 5. For the case of the Pt as-deposited and un-annealed structure with phosphorus implant (Fig. 4a), the 50 nm Pt layer resides on top of the implanted region and no apparent intermixing between the Pt and Ge is observed. The phosphorus distribution has a projected range of 25 nm, while the integration of the depth profile was set to provide the accurate dose of 2×10^{15} ions/cm². In the case of the 2 min annealed sample (Fig. 4b), it is evident that strong intermixing effects had occurred during annealing. Ge starts to diffuse towards the Pt layer and Pt diffuses into Ge, and their reaction forms the Ge_xPt_y phases. The platinum germanide layer was estimated to be around 58 nm, while the remaining Pt layer

Table 1
Identification of platinum and platinum germanide XRD peaks of Fig. 2a and b.

XRD peak	Diffraction	XRD peak	Diffraction	XRD peak	Diffraction	XRD peak	Diffraction
A1	Ge (200)	B1	Ge_3Pt_2 (301)	C1	Ge_3Pt_2 (201)	D1	GePt (100)
A2	Pt (100)	B2	Ge_2Pt_3 (041)	C2	Ge_3Pt_2 (301)	D2	GePt (020)
A3	Pt (200)	B3	Ge_2Pt (011)	C3	Ge_3Pt_2 (401)	D3	Ge_2Pt (011)
		B4	Ge_2Pt (200)	C4	Ge_2Pt (011)	D4	Ge_3Pt_2 (312)
		B5	GePt (220)	C5	Ge_2Pt_3 (060)	D5	$GePt_2$ (300)
		B6	Ge_2Pt_3 (313)	C6	Ge_2Pt_3 (213)	D6	GePt (130)

Fig. 3. XRD spectra of the germanidation process after annealing of ion implanted germanium substrates deposited with a 50 nm Pt layer. Annealing temperature 350 °C for 2 and 20 min (a) phosphorus and (b) boron implanted Ge samples, respectively.

on top of the structure, doped with Ge, has a thickness of 26 nm. The phosphorus distribution showed a double peaked distribution with maxima near the boundaries of the Ge_xPt_y layer. The highest phosphorus concentration resides deep within the $\text{Ge}_x\text{Pt}_y/\text{Ge}$ interface. This is attributed to the snow-plough effect according to which if the dopant has a limited solubility in the germanide, it will be expelled towards the boundaries of the formed germanide [29]. Annealing for 10 min (Fig. 4c), introduces into the top layer (20 nm thick) significant amounts of Ge which is transformed to platinum germanide. The Ge_xPt_y has an approximate thickness of 100 nm and the phosphorus segregates in the near-surface region, where it reaches a peak concentration of 10^{21} at/cm³. This comes through a reduction of the second peak at the $\text{Ge}_x\text{Pt}_y/\text{Ge}$ interface. Note also that there is a diffusion of Pt in the Ge substrate. As the annealing time increases further to 20 and 30 min (not shown here) the same trends are observed. The P distribution shows only one peak near the surface region (of the order of 10^{21} at/cm³), while the second peak is substantially flattened. Integration of the depth profile indicates that no significant dopant loss takes place. The overall phosphorus profile at long annealing times appears flat with an extended tail.

The corresponding evolution of the SIMS profiles in the case of the boron implanted samples is presented in Fig. 5. In Fig. 5a, the Pt as-deposited and un-annealed structure shows that the projected range of the boron atoms is 33 nm, without any diffusion or inter-mixing of boron, platinum and germanium. These effects occur after 10 min annealing at 350 °C, as can be observed in Fig. 5b. Ge diffuses into the Pt layer and platinum into Ge substrate. In addition, boron starts to diffuse into the Pt layer, while no signifi-

Fig. 4. P, Ge and Pt depth profiles of the phosphorus implanted samples determined by SIMS. (a) After the deposition of Pt without annealing. After annealing at 350 °C for 2 min (b), 10 min (c) respectively. All panels have the same range of left and right axes. The dotted vertical lines indicate the boundaries between the Pt or the Pt germanide and the Ge substrate.

Fig. 5. B, Ge and Pt depth profiles of the boron implanted samples. (a) After the deposition of the platinum layer without annealing. After 10 min annealing (b), and after 30 min annealing both at 350 °C. All panels have the same range of left and right axes. The dotted vertical lines indicate the boundaries between the Pt or the Pt germanide and the Ge substrate.

Fig. 6. J–V characteristics of the fabricated junction diodes as a function of the annealing time at 350 °C. (a) p⁺/n diodes, and (b) n⁺/p diodes. Diode area 50 × 50 μm².

cant redistribution takes place into the Ge substrate. The special features of the three elements depth profiles suggest that the Pt layer has not been transformed to platinum germanide. However, after the 30 min annealing at 350 °C significant changes in the depth profiles can be observed (Fig. 5c). Boron diffuses strongly towards the surface forming a small peak around 50 nm near into the Ge substrate. Overall, the boron profile is rather flat from 50 to 150 nm having a box-like shape. In addition, strong diffusion of Pt into the substrate and Ge towards the surface takes place. This is attributed to the formation of the platinum germanide, with a thickness around 100 nm.

The above presented SIMS results are particularly important since they reveal that the process of germanidation occurs via the parallel action of Pt diffusion into the Ge substrate and that of Ge diffusion into the remaining platinum layer. In addition, SIMS results are in line with the corresponding XRD measurements. In the case of phosphorus implanted samples, significant diffusion effects of all elements sets in during early stages of the 350 °C annealing leading to the fast formation of the platinum germanide and to phosphorus redistribution, which could be related to the damage produced by P implantation. For annealing times up to 10 min the phosphorus distribution has two peaks which tend to reside at the boundaries of the newly formed platinum germanide layer. These findings suggest that annealing at 350 °C should be limited in time. For the boron implanted samples the corresponding diffusion effects initiate after a 10 min anneal at 350 °C and proceed slowly to the formation of a platinum germanide at 30 min time during which boron also redistributes. The slow rate of the platinum germanide formation of the p⁺/n as compared to the case of the n⁺/p junctions is attributed to the lack of extensive ion implantation damage by the boron ions, which inhibits the fast

intermixing of B, Pt and Ge elements. In addition, B and Pt profiles exhibit a parallel movement into the Ge substrate which indicates an interdependent effect. A possible explanation can be drawn from the well established behavior of copper in p⁺ germanium layers [33,34]. If platinum diffuses into Ge via its interstitial form (Pt_i) we could expect a solubility enhancement of Pt_i in the p⁺ layer, as in the case of interstitial Cu [33]. An increase of the solubility could lead to precipitation or gettering effects of platinum in the p⁺ Ge layer [34,35]. In parallel, a retardation of Pt diffusion may take place as has been shown for the case of copper [33].

3.3. Electrical characteristics

Fig. 6a shows the J–V characteristics of the fabricated p⁺/n junctions of 50 × 50 μm² area. The Pt as-deposited and un-annealed diode showed a clear rectifying behavior, dominated by a series resistance at bias larger than 0.4 V and a forward to reverse ratio (I_F/I_R) of 5×10^4 between –2 and 1.5 V. The plateau region above 1 V arises from the instrument limitation and corresponds to a current density of 400 A cm^{–2}. The rectifying behavior of the non-annealed samples suggests that the implanted boron atoms occupy substitutional lattice sites as already suggested. The series resistance problem arises partially from the non-activated boron atoms and from the ion-implantation induced defects. The main influence of annealing in p⁺/n junctions at 350 °C is the gradual reduction of the series resistance. Neither the reverse current nor the diode exponential current depend on annealing. After 10 min at 350 °C the I_F/I_R ratio increases slightly to 7×10^4 between –2 V and 0.67 V (see Fig. 6a).

The J–V characteristics of the n⁺/p diodes are presented in Fig. 6b. Unlike the p⁺/n case, the Pt as-deposited and non-annealed structure exhibits a clear non-rectifying behavior. This ohmic behavior implies a low Schottky barrier and a p-type conductivity of the phosphorus implanted region. After annealing for 2 min at

Fig. 7. The experimental forward J–V characteristics were fitted to extract the basic parameters of the diodes. Both panels show the good quality of the fitting. (a) p⁺/n and (b) n⁺/p diodes.

350 °C, the J–V characteristics showed rectifying behavior with an I_F/I_R ratio of 6×10^3 between 2 and –0.69 V. This low ratio results from the high reverse current. Further annealing at 350 °C deteriorates severely the reverse current, and increases slightly the series resistance of the structure. It should be mentioned that the current of both the p⁺/n and n⁺/p diodes do not scale either with area or with perimeter, which indicates that the measured current is composed from bulk and perimeter components.

The forward characteristics of the above presented n⁺/p and p⁺/n diodes were further analyzed in order to extract the ideality factor n and the series resistance R_s of the diodes. The analysis was based on the following equation which approximately describes the diode characteristics in the forward region of operation [36]:

$$I = I_0 \left[\exp \left[\frac{q(V - IR_s)}{nkT} \right] - 1 \right]$$

where I_0 is the diode saturation current, and V is applied diode voltage. The quality of the fitting is shown in Fig. 7 for both n⁺/p and p⁺/n diodes. The ideality factor n approaches 2 when recombination current dominates and 1 when the diffusion current dominates. In the case that the two current components are comparable between each other, n has a value between 1 and 2. The I–V characteristics were fitted with adjustable parameters R_s , n and I_0 . The dependence of the extracted ideality factor of both diode types upon the annealing time are presented in Fig. 8a. For n⁺/p diodes n fluctuates around 1.3, while for p⁺/n diodes it was found around 1.2. This result clearly

Fig. 8. Ideality factor (a), series resistance (b), and forward to reverse current ratio I_F/I_R (c), as a function of the annealing time at the temperature of 350 °C. The above parameters were extracted from the fitting procedure of the forward current characteristics. (Error bars in Fig. 8a for N⁺P at 2 and 5 min are very small).

indicates that the dominant contribution originates from the diffusion current. In addition, the contribution of the recombination current is larger in the case of n⁺/p diodes. The diode series resistance as a function of annealing time is presented in Fig. 8b. As the annealing time increases, the n⁺/p diodes series resistance increases steadily from 36 to 112 Ω after 30 min. For the case of p⁺/n diodes the main influence of annealing occurs during the first 10 min and the R_s saturates to 43 Ω after 20 min. Finally, Fig. 8c shows the evolution of the I_F/I_R ratio with annealing time.

The relatively high ideality factor in both diodes signifies an increased participation of the recombination current and is attributed to the unpassivated surface states. The higher ideality factor which characterizes the n⁺/p diodes is attributed to the effect of Pt diffusion within the depletion region of the diode. As SIMS analysis indicated Pt diffuses deeper within the germanium substrate in the case of the phosphorus implanted samples as compared to the boron implanted ones. Usually, the introduction of metal atoms within the depletion region of device induces point defects with one or more deep energy states which act as generation–recombination centers [37]. Point defect activity has been detected in the C–V and G–V characteristics and will be discussed later. Therefore, the presence of Pt related defect states within the depletion region can explain both the higher ideality factor and the high reverse current of the n⁺/p junctions. On the contrary, the diffusion of Pt

Fig. 9. Admittance characteristics recorded from selected diodes of the study. C–V characteristics (a) and the corresponding G–V characteristics (b) of n⁺/p diodes. These clearly indicate the presence of Pt-related defects for the case of 350 °C annealing while no such defects were observed for the 300 °C annealing case. (c) C–V characteristics of p⁺/n diodes where no evidence of gross contamination was observed.

Fig. 10. J–V characteristics of the fabricated junction diodes as a function of annealing time and temperature. (a) p^+/n diodes and (b) n^+/p diodes. Diode area $50 \times 50 \mu\text{m}^2$.

in the boron implanted germanium is rather limited and it is always enclosed by the boron distribution. The increase of the series resistance with annealing time of the n^+/p junctions is attributed to the reduction of the phosphorus concentration at the platinum germanide/germanium interface. For the case of p^+/n junctions, the significant reduction of the series resistance with annealing time occurs during the first 10 min where limited germanide formation occurs. This is attributed to the reduction of the ion-implantation induced defects and to the better contact resistance between the germanide and the germanium layers.

The C–V and the G–V characteristics of the n^+/p junctions revealed clearly the presence of defect states in the depletion region when a 350 °C annealing temperature is used. Fig. 9a shows the C–V characteristics recorded from three n^+/p junctions that were annealed at 350 °C for 1 min (curve a) 350 °C for 2 min (curve b) and 300 °C for 10 min (curve c). The corresponding G–V characteristics are presented in Fig. 9b. Annealing at 350 °C, for 1 min is too short and cannot remove the implantation induced defects. Indeed, the C–V characteristic shows an enormous hump extending from 0 up to –4 V. The corresponding G–V characteristic shows an asymmetric intense peak at the same voltage region. After a 2 min annealing at 350 °C, the C–V characteristic shows a small hump below –1 V, which is observed only if the diode has been brought previously into the forward region of operation. The G–V characteristic also shows a clear loss peak which implies the presence of hole trap. Longer annealing times above 2 min at 350 °C (not shown) increase this characteristic hump, which now appears as a peak in the C–V characteristic. These findings are in agreement with the J–V characteristics (Fig. 6b) and suggest that the defect activity could be attributed to Pt-related defects. On the contrary

after annealing at lower temperature at 300 °C for 10 min no humps or loss peaks are observed in the C–V or the G–V characteristics (Fig. 9a and b). This finding is very important since: (a) it suggests that the lower temperature annealing at 300 °C is low enough to confine the fast Pt diffusion within the heavily n^+ region of the diode preventing thus the formation of Pt-related generation–recombination centers within the depletion region; and (b) it is sufficient to eliminate the phosphorus implantation induced damage via the germanide formation. The C–V characteristics of the p^+/n junctions as a function of the annealing time at 350 °C are shown in Fig. 9c. In this case no significant evidence of gross Pt-related contamination was observed.

We must point out here that usually metallic contamination of the depletion region, introduces acceptor-like traps which do not respond in p-type Ge [30]. Early reports showed that Pt introduces in n-type Ge deep electron traps at $E_c-0.17$ eV and at $E_c-0.21$ eV [38]. For example, recent studies on Pt germanidation of n-type Ge using rapid thermal annealing at the temperature range of 300–500 °C indicate a small concentration of electron traps which are attributed not to Pt contamination but rather to Ar ion sputtering damage [39]. In addition, using higher germanidation temperature up to 650 °C, Pt indiffusion is not so evident and the observed deep states are attributed to Cu contamination [40]. The observation of defects states only in p-type germanium (n^+/p diodes) may indicate the formation of Pt-complex defects.

Fig. 10 shows the J–V characteristics from the second split of samples which have been annealed either at 300 or at 350 °C. Regarding the p^+/n junction, annealing has a small influence on the reverse current, which increases at longer annealing times at 300 °C. For the case of n^+/p diodes annealing at 300 °C for 10 min provide the best characteristics of this study. The forward current reaches the instrument limit of 400 A/cm² at –0.72 V, with a rather flat reverse current and a I_F/I_R ratio of 1.6×10^4 .

4. Discussion and conclusions

It is well known that low-temperature annealing of transition metals such as Pd, Ni, Co, Pt deposited on germanium leads to the formation of germanides [28,30]. In the case of amorphous germanium films (α -Ge), annealing continuation results to crystallization of the α -Ge film, the so-called metal induced crystallization process (MIC) [30,31]. According to a possible scenario, after the formation of the germanide, metal atoms or germanide nodules continue to diffuse into the α -Ge [30,31]. The driving force for this movement is the minimization of the energy of the diffusing species. Ge atoms which stay behind attach to the germanide template and form crystalline germanium. The crystallization process induced by the transition metals brings a significant reduction of the crystallization temperature which depends on the choice of the metal and it closely related to the diffusivity of the metal [30]. In addition, when dopant atoms are present in the α -Ge, the process of crystallization is accompanied by the metal induced dopant activation (MIDA) effect [32]. In a different scenario [41–45] for MIC, when a metal is deposited on Ge (crystalline or amorphous) and subsequently heated close to—but lower than—the eutectic temperature of the metal–Ge alloy, the Ge is dissolved inside the metal. Then, during cooling down, the solubility of Ge is decreased which favors the flow of excess Ge from the metal to the substrate resulting in crystalline, epitaxial Ge (MIC) on top of the Ge substrate. Again, during this MIC process any dopants present could be substitutionally incorporated to the crystallizing Ge resulting in MIDA.

Within the MIDA context J.H Park et al. [26], demonstrated high performance p^+/n and n^+/p Ge diodes formed at 380 °C, using 5 nm of cobalt deposited on top of a boron or a phosphorus implanted

region. The diode characteristics showed high forward current density (221 A/cm^2 and 135 A/cm^2 at rather high bias $|V_f| = 2 \text{ V}$ for the n^+/p and the p^+/n respectively) with a $\sim 2 \times 10^4 I_F/I_R$ ratio. These characteristics were attributed to the MIC and the MIDA effects. Nishimura et al. [27], demonstrated the activation of phosphorus atoms in Ge substrates at a temperature of 300°C using 50 nm of nickel also deposited on top of a phosphorus implanted region. The proposed model in this case was the snow-plough effect in combination with MIC. During the low-temperature annealing process, the formation of nickel germanide led to the segregation of the dopant at the NiGe/Ge interface due to the lower solubility of the dopant within the formed germanide.

In this work we demonstrate the fabrication of high performance n^+/p and p^+/n germanium junction diodes using low-temperature annealing within the range of $300\text{--}350^\circ\text{C}$, in the presence of a top platinum layer. A Pt MIDA process may be effective in our case to obtain the dopant activation and the diode rectification properties at this very low annealing temperature. The choice of platinum was based on the low diffusivity in Ge, which is lower than that of Ni and Co, in order to limit the diffusion of Pt within Ge and thus the contamination of the diode depletion region [30,31]. The presented J–V characteristics indicate high forward currents, independent of the diode type that can reach 400 A/cm^2 at low forward bias of 0.7 V which takes full advantage of Ge as a high mobility channel material suitable for high performance/low operating power applications. In the case of n^+/p junctions the germanidation rate is fast at 350°C , assisted probably by the phosphorus implantation damage, where the phosphorus piles up at both germanide interfaces for short annealing times. The experimental evidence from SIMS suggests a snow plough mechanism of the phosphorus concentration, where for small annealing times segregation close to the Pt-germanide/Ge interface is observed. This may cause a reduction in the electron Schottky barrier width at the Pt-germanide/Ge interface which could explain the decrease of series resistance. During longer annealing, the phosphorus segregates near the top surface reducing the dopant density at the Pt-germanide/Ge interface, which is consistent with the observed increase in the series resistance. In addition, at longer annealing times, severe Pt-related contamination is induced within the depletion region of the diodes. Annealing at lower temperatures and longer times (300°C , 10 min) restricts these unfavorable effects and results to n^+/p with better characteristics. We must also notice that no particular measures were taken in order to reduce the surface current component. In the case of p^+/n diodes the germanidation rate is slow and it requires $350^\circ\text{C}/30 \text{ min}$ to completely transform the Pt layer into a germanide layer. In this case the lower annealing temperature at 300°C for 10 min is sufficient to reduce both the implantation damage and to improve the series resistance of the diodes.

In conclusion, the presented results demonstrate that using platinum assisted low temperature dopant activation at 300°C the n^+/p diodes outperformed the conventionally activated diodes. In comparison to the Ni and Co assisted dopant activation higher forward currents were accomplished at lower bias. The MIC/MIDA effect may be responsible for dopant activation at low temperature while the observed snow-plough effect in n^+/p diodes may be responsible for the low series resistance. Finally, the low diffusivity of Pt during the germanidation process limits the metallic contamination of the diode depletion region, especially when the lowest annealing temperature of 300°C is employed. Pt assisted dopant activation appears as a promising approach for the formation of high performance Ge junction diodes.

Acknowledgement

This work was partly supported by the European FP7 ICT project DUALLOGIC-214579.

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