Organic Electronics 15 (2014) 904–912

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Letter

Variation-based design of an AM demodulator in a printed complementary organic technology

S. Abdinia [a,*], F. Torricelli [a,1], G. Maiellaro [b,2], R. Coppard [c], A. Daami [c], S. Jacob [c], L. Mariucci [d], G. Palmisano [b], E. Ragonese [b], F. Tramontana [e], A.H.M. van Roermund [a], E. Cantatore [a]

[a] Eindhoven University of Technology, Department of Electrical Engineering, MSM, Eindhoven, The Netherlands
[b] University of Catania, DIEEI, Italy
[c] CEA-LITEN, Grenoble, France
[d] CNR-IMM, Rome, Italy
[e] STMicroelectronics, Catania, Italy

ARTICLE INFO

Article history:
Received 27 August 2013
Received in revised form 27 January 2014
Accepted 28 January 2014
Available online 11 February 2014

Keywords:
Printed OTFTs
AM demodulator
Amplifiers
Envelope detector
Monte Carlo simulations
Parametric variations

ABSTRACT

In this work, the design of a high-frequency AM demodulator in a printed complementary organic technology is presented. The behaviour and the variability of printed circuits are predicted by means of accurate transistor modelling, statistical characterization, and Monte Carlo simulations. The effectiveness of the design approach is readily verified by comparing measurements and simulations of simple digital blocks as well as two differential amplifiers. These amplifiers can be used as continuous-time comparators in the demodulator. In addition, the possibility of high-frequency rectification using the printed organic TFTs is shown by providing the experimental results of an envelope detector measured under different load and input conditions. All the measurements are performed in air. Finally, the simulation of a complete AM demodulator system including the measured blocks is demonstrated.

© 2014 Elsevier B.V. All rights reserved.

1. Introduction

Organic electronics is a promising field for the implementation of novel large-area applications on flexible substrates, including Radio Frequency Identification tags (RFIDs) [1,2], smart surface sensors [3], and actuators [4]. However, the relatively high variability in the characteristics of Organic Thin Film Transistors (OTFTs) makes it very challenging to have a robust design [5,6]. The global and local variations in the organic devices and the defects in the process lead to soft faults (deviation from the desired performance) and hard faults (failure to function) at the circuit level, respectively. Such shortcomings, which are a consequence of the chosen low-temperature and low-cost techniques, are seriously limiting the integration of organic circuits. In the case of unipolar technologies, the lack of n-type transistors further exacerbates the robustness issues. Although dual-gate transistors have been demonstrated to improve circuit robustness [7], the use of a complementary technology along with a design approach able to take into account the technology variability is the most promising route to further improve the complexity of both analogue and digital circuits [8,9].

The widespread use of organic electronics applications for a substantial improvement in the quality of everyday life could be fostered by the advancement of printing organic technology, due to its high throughput and potentially low cost [10,11]. However, the above-mentioned large variation of parameters in organic transistors becomes even more noticeable in printing technologies, due

* Corresponding author. Tel.: +31 402473407.
E-mail address: s.abdinia@tue.nl (S. Abdinia).
[1] Present address: University of Brescia, Department of Information Engineering, Brescia, Italy.
[2] Present address: STMicroelectronics, Catania, Italy.

http://dx.doi.org/10.1016/j.orgel.2014.01.021
1566-1199/© 2014 Elsevier B.V. All rights reserved.

to the low degree of spatial correlation which is intrinsic in printing processes. That is why circuits implemented based on printed OTFTs [9–14] are mainly limited to digital electronics or large-area switch matrices.

Another important challenge for OTFTs is the high frequency (HF) performance and rectification efficiency needed by applications such as RFIDs. Indeed, working at frequencies above a few megahertz is very challenging for organic TFTs, since mobility typically does not exceed 0.5–1 $cm^2/V\,s$ [15,16]. Moreover, the typical high threshold voltage of OTFTs greatly impacts the rectifier Power Conversion Efficiency (PCE). State-of-the-art rectifying organic diodes adopt either vertical Schottky diodes [17] or diode-connected OTFTs [16]. The former provide the best performance in terms of operating frequency thanks to the very thin organic semiconductor layer. The latter are preferred when the rectifying diode has to be embedded in a complete RFID system, as it avoids specific technology steps and reuses the OTFTs. However, in this case diode performance is affected by the large channel length [16].

In this work, we present the design of a demodulator for amplitude-modulated (AM) radio signals, which is printed on a plastic substrate using a complementary organic technology. The circuit design and simulations are based on accurate modelling of p-type and n-type TFTs. Measurements of fundamental digital blocks such as inverters and NAND gates verify the model, and Monte Carlo (MC) simulations give an estimation of the effect of the technology parameter spread on circuit performance. The measured high frequency envelope detector and continuous-time comparators can be directly combined to make a demodulator operating at 13.56 MHz. The simulations of the complete AM demodulator system confirm its functionality and give suggestions for further improvements in the circuit design as well as in the OTFT modelling.

2. Modelling and simulations

2.1. OTFT model

The OTFTs are implemented in a top-gate bottom-contact structure, using a polytriarylamine (PTAA) derivative for p-type and an acene-based diimide for n-type semiconductors. The typical mobility of n-type and p-type OTFTs is 0.023 $cm^2/V\,s$ and 0.025 $cm^2/V\,s$, respectively. More details on the process can be found in [13].

The proposed OTFT model considers the static behaviour, the parasitic capacitances, and the parametric variability due to the printed technology. A physically based compact model [18] was used to fit the measured transfer and output characteristics of both p-type and n-type staggered transistors. The model takes into account the channel behaviour as well as the contact effects. According to the electrical measurements of long channel transistors, the drain current is a power law of the gate-source potential and the channel transport is modelled assuming an exponential distribution of traps in the semiconductor. Hence, when the transistor operates in accumulation (i.e., above threshold), the current expression reads [19,20].

$$I_D = \frac{W}{L}\left[G_t\left(V_A^{\gamma t} - V_B^{\gamma t}\right)\left(1 + \frac{|V_{DS} - V_c|}{L \times E_p}\right) + \frac{V_{DS}}{R_{\text{off}}}\right] \tag{1}$$

where W and L are the channel width and length, respectively, G_t is a pre-factor dependent on physical and geometrical parameters (temperature, energetic disorder, charge spatial localization, and gate-insulator capacitance), γ_t is related to the disorder in the organic semiconductor, E_p takes into account the channel length modulation, and R_{off} considers the bulk current related to unintentional doping in the organic semiconductor.

When the transistor works in the sub-threshold regime, the measured drain current increases exponentially with the gate voltage. Such a behaviour could be attributed to deep trap states [21]. The above-threshold and the sub-threshold regimes are combined according to the interpolation function presented in [22]:

$$V_A = V_{ss} \ln\left[1 + \exp\left(\frac{V_{GS} - V_c - V_T}{V_{ss}}\right)\right] \tag{2}$$

$$V_B = V_{ss} \ln\left[1 + \exp\left(\frac{V_{GS} - V_{DS} - V_T}{V_{ss}}\right)\right] \tag{3}$$

where V_{SS} is the sub-threshold slope, V_C is the voltage drop at the source injecting contact, and V_T, V_{GS}, V_{DS} are the threshold voltage, the gate-source voltage, and the drain-source voltage, respectively.

Electrical characteristics of p-type OTFTs with a channel length ranging from 200 μm to 20 μm scale with the transistor channel length, and are accurately modelled with Eqs. (1)–(3). This suggests that the channel transport is the dominant physical mechanism. On the contrary, the electrical characteristics of n-type OTFTs do not scale with the transistor channel length. Indeed, the normalized drain current of a transistor with L = 20 μm is lower than that of a transistor with L = 200 μm. This experimental behaviour suggests that contact effects [23,24] are limiting the current. The contact resistance in these transistors is mainly related to the limited injection at the source contact induced by the presence of a reversed biased Schottky diode, the conductivity of which is strongly modulated by the gate bias. The current injected by the source contact as a function of the gate and drain potentials is modelled as in [25]:

$$I_c = WI_0 \exp\left(4\sqrt{\frac{|V_c + V_c|}{2V_{00}}}\right)\left[1 - \exp\left(-\frac{V_c}{V_n}\right)\right] \tag{4}$$

where $I_0 = I_{00}\left(1 + \left(\frac{|V_{GS}|+V_{GS}}{2}\right)^{\gamma c}\right)$ and V_{00}, V_n, I_{00}, and γ_c are the contact parameters. The electrical characteristics of n-type OTFTs are modelled as the series of an "ideal transistor" and a reverse biased Schottky diode. Therefore, p- and n-type transistors have the same channel model, while only for n-type transistor is the contact resistance also needed.

Fig. 1(a) and (b) shows the measured (blue symbols) and modelled (red lines) characteristics of n-type and p-type transistors with dimensions (W/L) equal to $1000\mu/20\mu$. The transfer characteristics (left panels) are given for two different V_{DS}, 1 V and 40 V, and the output characteristics (right panels) are shown for three different V_{GS}, namely

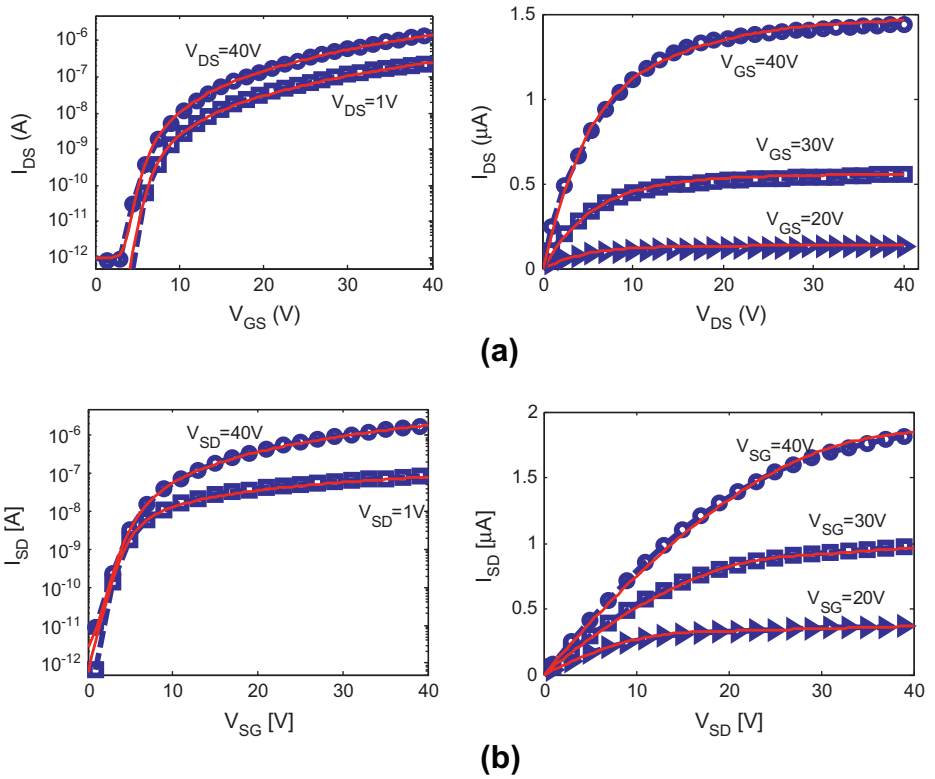

Fig. 1. Measured (blue symbols) and modelled (red line) transfer and output characteristics of (a) n-type and (b) p-type transistors ($W/L = 1000\mu/20\mu$) (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.).

20 V, 30 V, and 40 V. In all the cases the model is in agreement with the measurements. It is worth noting that the n-type OFETs show lower saturation voltage than the p-type ones, even if the threshold voltage parameter (see Table 1) is nearly the same. This is due to the parasitic contact resistance, which causes a voltage drop at the injecting contact (source), thus reducing the overdrive voltage of the OFET and lowering the saturation voltage.

To evaluate the total source-drain capacitance (C_{tot}) of transistors with different channel lengths, a set of capacitance measurements were also carried out on the multi-finger OTFTs at different V_{GS} biases. The layout of a multi-finger transistor with four channels ($n = 4$) is shown in Fig. 2, where L is the channel length, W is the total channel width, and E_{G-SD} is the overlap of gate layer on source/drain fingers. Based on the measurements, the following empirical formula was used in the model to take

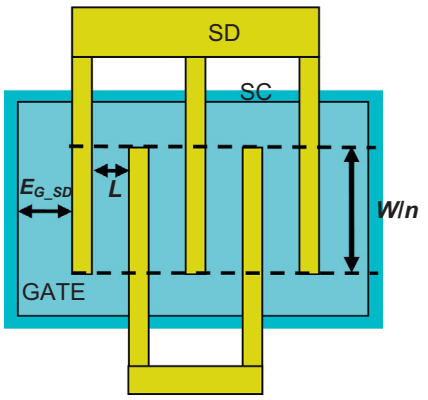

Fig. 2. Layout of a multi-finger transistor with 4 channels ($n = 4$). SD and SC refer to source/drain and semiconductor, respectively.

Table 1
The nominal value and standard deviation (σ) of OTFT parameters.

	Symbol	Channel parameters						Contact parameters			
		G_t (S/cm)	γ_t	E_p (V/μm)	R_{off} (Ω)	V_T (V)	V_{ss} (V)	V_{00} (V)	V_n (V)	I_{00} (A/μm)	γ_c
N-type OTFT	Nominal value	7.75e−13	3.39	0.1	2e15	5.4	1	35	2.86	64.17e−16	3.5
	Σ	2.73e−13	0.5	–	–	1.55	0.12	–	–	–	–
P-type OTFT	Nominal value	2.01e−11	2.01	10	5e14	3.69	1	–	–	–	–
	Σ	8.9e−12	0.1	–	–	0.3	0.13	–	–	–	–

the effects of the transistors' parasitic capacitance into account in dynamic simulations:

$$C_{tot}(L) = C_{tot}(0) + C_{ox}L[W + 2(n-1)E_{G-SD}] \quad (5)$$

where the first term, $C_{tot}(0)$, is the overlap capacitance obtained when $L = 0$ μm, while the second term is the contribution of the channel to the capacitance. Since the transistors have a multi-finger structure, the calculated capacitance was divided between source and drain, depending on the number of fingers at each side. It is worth noting that this formula is valid only when the device is in the accumulation regime.

Because of the parametric variability in printed OTFTs, statistical characterization is crucial for having a reliable estimation of circuit functionality. That is why in this work, in addition to the explained compact model, a statistical model is employed. The variability of four transistor channel parameters, namely G_t, γ_t, V_T, and V_{ss}, were extracted from a set of measured devices. These parameters correspond to the transistor's electrical characteristics including mobility, threshold voltage, and sub-threshold slope. The obtained data are used to run Monte Carlo (MC) simulations based on uncorrelated Gaussian parameter variations, within the limits derived from the OTFT measurements. The results of nominal and statistical simulations of the circuits based on this model are presented in the following sections. Table 1 gives the nominal value of the model parameters and their standard deviation (σ).

2.2. Circuit simulation

To validate the reliability of the model, measurements of two logic gates are compared with their nominal simulations in Fig. 3. These digital building blocks, namely an inverter and a NAND gate, are the components needed to realize any combinatorial and sequential logic circuit in relevant applications such as RFID tags. The inverter was measured at two different supply voltages, V_{dd} = 20 V and 40 V (Fig. 3(a)). The nominal trip point voltage (V_{trip}) of the inverter with equal width for p-type and n-type transistors is 11 V at V_{dd} = 20 V and 19.3 V at V_{dd} = 40 V, which guarantees a good static noise margin. The NAND was measured at V_{dd} = 40 V with one input (in Fig. 3(b), A) set at 40 V and the other (B) swept from 0 V to 40 V. In both inverter and NAND gate, there is a good agreement between simulated and measured performance of the circuits.

MC simulations using the statistical parameters in Table 1 were performed to study the effect of transistor parametric variability on printed organic circuits. Fig. 4(a) presents the results of 100 iterations of an MC simulation for the inverter, including the transfer characteristics and the histogram of V_{trip}. This shows that despite all the variations caused by the reduced control over the printing process, the inverter is functional in all the cases and its transfer characteristics are centred at $V_{dd}/2$, leading to a high noise margin. Fig. 4(b) depicts the results of a similar simulation for another version of the printed technology that aims at a better performance [26–28] at the expense of higher variation risk.

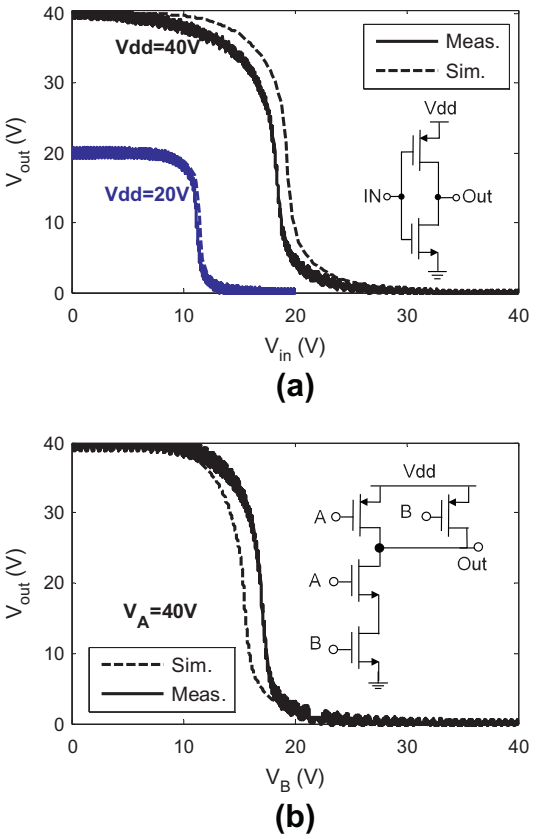

Fig. 3. Measurements vs. simulations of digital building blocks (a) inverter at V_{dd} = 20 and 40 V (W_p/W_n = 1); (b) NAND gate at $V_A = V_{dd}$ = 40 V.

The measurements and simulations illustrated in this section show that the model can well predict the behaviour of the circuits, and the slight difference between measurements and simulations can be explained by process tolerances. Therefore, it can be concluded that the physically based model for organic transistors incorporating the parameter variations can provide a reliable prediction of the behaviour of circuits manufactured in this complementary organic technology.

3. AM demodulator design

Demodulation is an enabling function in potential organic electronic applications such as RFID tags based on the standard "reader talks first" concept, where the RFID tags must have the capability to receive habilitation messages coming from the interrogator. The main building blocks of an AM demodulator, as shown in Fig. 5, are an HF envelope detector and a voltage comparator. The envelope detector extracts the low-frequency envelope from the high-frequency carrier, and the comparator converts the envelope signal in a full-swing output data stream, providing the demodulated signal.

In this section, two differential amplifiers that can be used as comparators for the AM demodulator circuit are

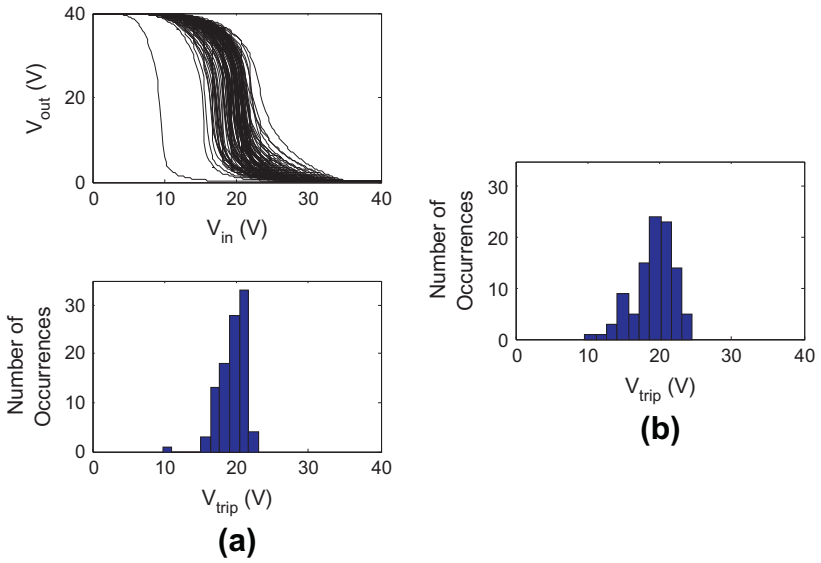

Fig. 4. (a) Inverter's transfer characteristics and trip point (V_{trip}) histogram generated by 100 iterations of MC simulation; (b) V_{trip} histogram for an inverter in [27] built in a different version of the printed technology [26], which aims at higher mobility but has larger variability.

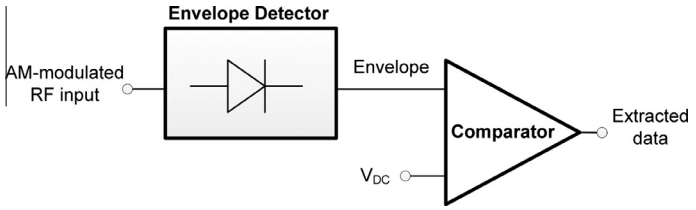

Fig. 5. Building blocks of a demodulator to recover an AM-modulated data.

presented. In addition, different measurements of an envelope detector employing a diode-connected OTFT as the rectifying device are demonstrated in order to show the feasibility of HF rectification using our printed OTFTs. Finally, the simulation of an AM modulator formed by combining these measured blocks is illustrated. Fig. 6 shows the picture of a foil containing all the implemented blocks.

3.1. Comparators

A simple differential amplifier with a current-mirror active load that can be used as a 1-stage comparator is shown in Fig. 7(a). The circuit was designed and measured by providing an external bias current of 0.3 μA. One of the inputs (V_{in+}) was set at a specific voltage and the other input (V_{in-}) was swept back and forth from 0 to 40 V. Fig. 7(b) shows the simulated and measured output for different values of V_{in+}, namely 15 V, 20 V, and 25 V. The amplifier shows a relatively good match between the transistors (little offset), although it has a hysteresis of about 1 V, due to instability of the OTFTs under bias. The simulated and measured amplifier gains for V_{in+} of 20 V are about 26 dB and 29 dB, respectively.

The two-stage architecture depicted in Fig. 8(a) can be used to achieve higher gain. The static and dynamic

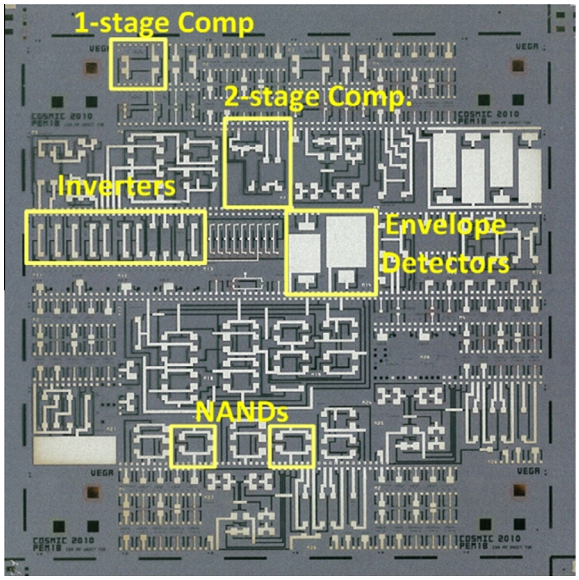

Fig. 6. Picture of a foil with different analogue and digital building blocks.

behaviours of the comparator were measured at 40 V supply voltage, 30 V common-mode voltage, and 0.15 μA

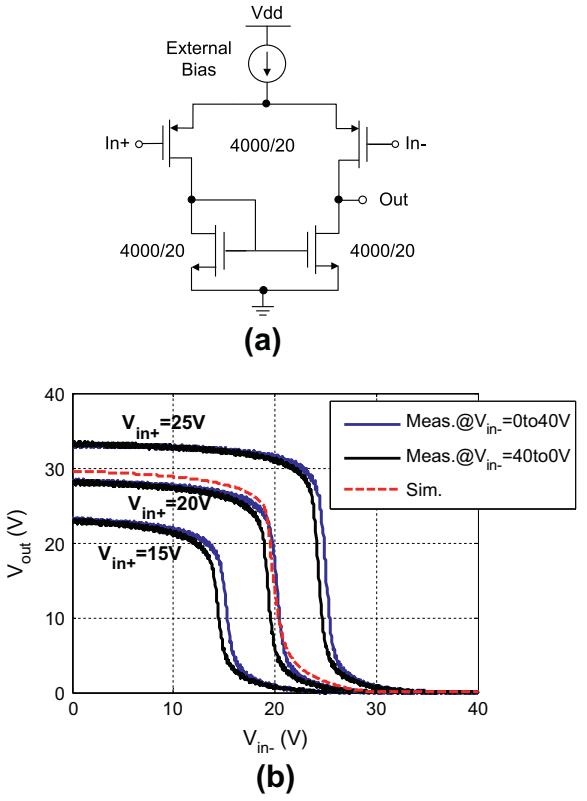

Fig. 7. (a) Schematic of the differential amplifier; (b) output voltage vs. input voltage (V_{in-}) at different V_{in+} values.

bias current. Fig. 8(b) shows the static measurements while the negative input (V_{in-}) was set at 30 V and the positive input (V_{in+}) was swept. A gain of 40 dB was achieved, which is 18 dB higher than the printed operational amplifier shown in [14], and 1 dB lower than the simulated gain (dashed line). The measured input offset in this case is 2 V. For dynamic measurements shown in Fig. 8(c), V_{in-} was set to 30 V and a 1 Hz pulse signal was applied to V_{in+}. The total load capacitance at the output node due to the measurement instruments was 37 pF.

3.2. Envelope detector

An envelope detector can be implemented with a rectifying device and an RC series load that is chosen according to the envelope frequency to provide a first-order low-pass filtering in the voltage domain. To investigate experimentally the HF performance of a rectifying device in our printed organic technology, we measured a diode-connected OTFT with an external load under different input and load conditions. A p-type transistor is preferred due to its better mobility. A minimum transistor length of 10 μm is used for better frequency behaviour, and the transistor width is fixed at 36,000 μm.

The adopted measurement setup for the rectifier characterization is shown in Fig. 9. Measurements were carried out on foil by means of a Cascade Summit 12,000 prober. The rectifier was tested in air at ambient temperature. The output voltage was measured by means of a semiconductor parameter analyser. The proposed setup was preferred to a resistive load configuration since it allows characterization for different input signal amplitudes at a constant load current (I_L). The rectifier performance was also explored at different input frequencies. A discrete C_L of 100 nF was used.

Fig. 10 shows the measured output voltage of the rectifier at different frequencies (100 Hz–13.56 MHz) and load currents (0–100 nA). In all the figures, the absolute value of the rectifier output voltage is shown. It is apparent how the rectifier performance degrades by increasing the frequency, regardless of the load current. A corner frequency of around 10 kHz can be estimated, above which a significant drop of the rectified voltage is experienced. A constant gate-source capacitance based on Eq. (5) and equal to 38 pF for the OTFT used in the rectifier was included in the model for the simulation. As illustrated in the figure, the low-frequency performance is well estimated by simulations, while the performance degradation at higher frequencies is still not predicted well by the model. The discrepancy between measurements and simulations at high frequencies could be attributed to a lowering of the effective mobility, due to a less efficient hopping transport when the time of flight in the OTFT channel is reduced.

To further evaluate the rectifier's performance at 13.56 MHz, we measured the output voltage for three different values of load current (I_L = 0 A, 10 nA, 100 nA) as depicted in Fig. 11. The rectified voltage drops by 10% and 18% when measured at 10 nA and 100 nA load currents, respectively. These results are obviously dependent on the transistor width. For both measurements of Figs. 10 and 11 the input signal has an average value $V_M = -25$ V, and a peak-to-peak value $V_{PP} = 30$ V. The characteristics of the rectifier are further explored in Fig. 12 which shows the rectifier output voltage for two different V_{PP} (15 V and 30 V) under an open-circuit condition (I_L = 0 A). The larger drop observed for increasing frequency when using the higher V_{PP} (30 V) may indicate that the low-frequency performance of the rectifier is limited by the OTFT threshold voltage. On the other hand, the similar output voltage at high frequency is compatible with a mobility-limited performance at HF.

Finally, the robustness and reliability of the adopted organic p-type TFT as rectifier was evaluated by comparing the DC characteristics before and after the large-signal AC measurements. Fig. 13 shows no appreciable degradation of the OTFT.

3.3. Simulation and discussion

A simulation was performed in order to study the functionality of the measured envelope detector and comparator when combined to form the AM demodulator of Fig. 5. This architecture uses an analogue amplifier to extract the data from an AM signal with reduced modulation depth, compared to [29], which employs a cascade of inverters and needs a modulation index close to 100%. The simulation results are shown in Fig. 14, where an 80-V_{pp} signal is applied to the input. A data rate of 10 Hz was chosen,

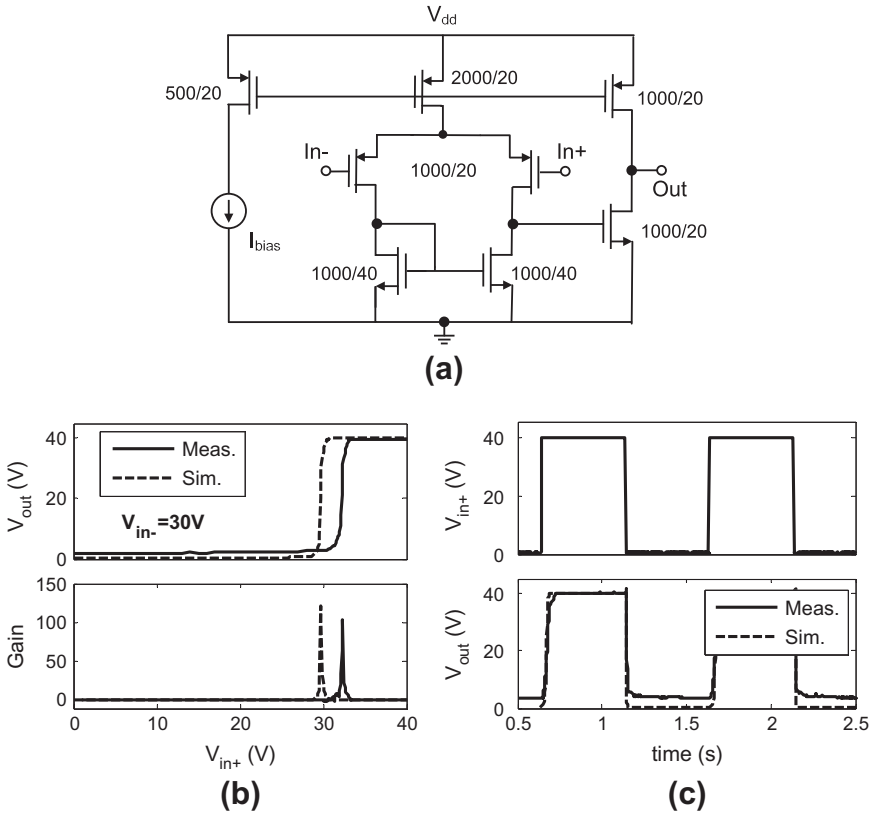

Fig. 8. (a) Schematic of the two-stage comparator; (b) static measurements and simulations; (c) dynamic measurements and simulations @ V_{in-} = 30 V, V_{dd} = 40 V, and I_b = 0.15 μA.

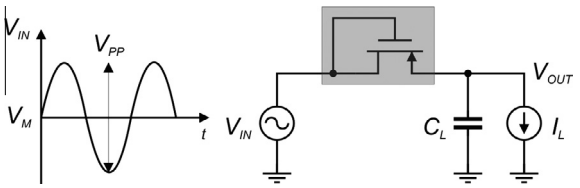

Fig. 9. Measurement setup of the rectifier/envelope-detector.

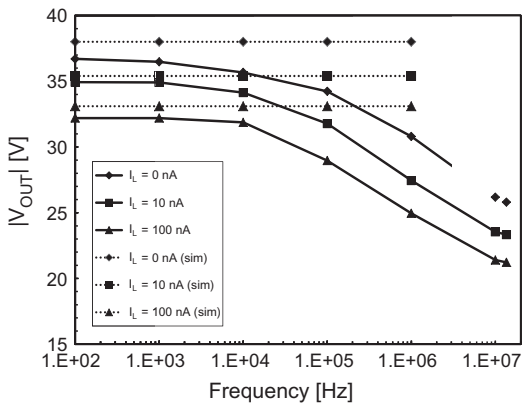

Fig. 10. Rectifier output voltage as a function of input frequency at different load currents (solid lines show measurement results and dashed lines show simulations).

which is reasonable based on comparator measurements. The carrier frequency for simulation was set to 10 kHz, since it is the highest frequency at which the simulation and measurements of the envelope detector are in close agreement. At this frequency, a modulation index of 30% is large enough to surpass the offset of the comparator and achieve correct functionality. The lowest graph of Fig. 14 shows the outputs of both 1-stage and 2-stage comparators under this modulation depth. At the high frequencies needed for practical applications, the performance of the envelope detector degrades and an increase of the modulation index would be required. To avoid the need to increase the modulation index, which is inconvenient from the point of view of the reading distance and requires large DC storage capacitors on the tag, it is necessary to improve the circuit performance. From the technology perspective, this can be done by increasing the OTFT mobility and lowering its threshold. From the circuit perspective, the negative effect of the threshold voltage on the envelope detector can be reduced using rectification schemes including threshold cancellation. The offset in the comparator can be also reduced for example using auto-zeroing techniques. To further study the performance of the circuits for practical applications at HF, a model that takes into account the effects of charge transport characteristics

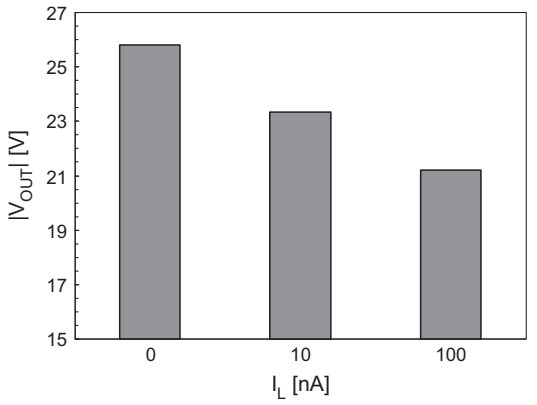

Fig. 11. Rectifier output voltage as a function of load currents at 13.56 MHz input frequency.

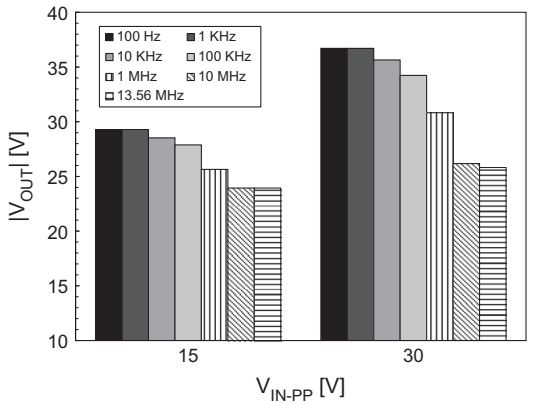

Fig. 12. Rectifier output voltage as a function of input signal amplitudes for different input frequencies.

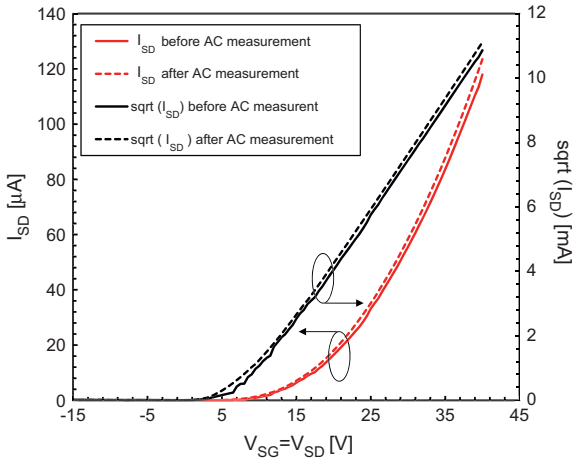

Fig. 13. Diode DC characteristics before and after large-signal AC measurements.

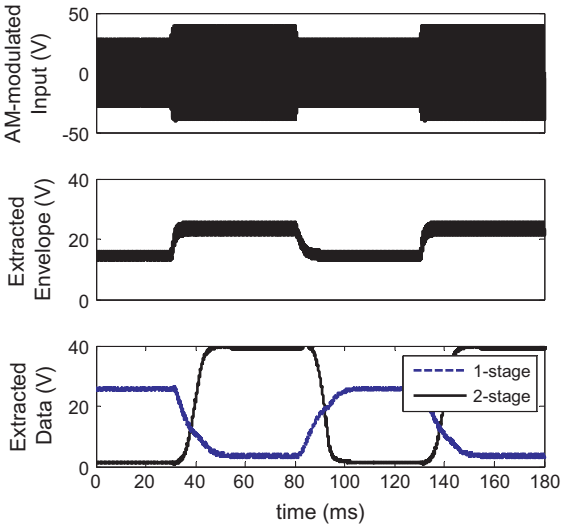

Fig. 14. Simulation of the AM-demodulator (Fig. 5) using the designed and measured building blocks, $f_{carrier}$ = 10 kHz, f_{data} = 10 Hz, modulation index = 30%.

on high-frequency performance of OTFTs needs to be developed.

4. Conclusion

In this work we present a design flow for a printed complementary organic technology that we used to design an AM demodulator, a bottle-neck block in RFID tags and similar applications. The availability of well-modelled analogue and digital circuits along with high-frequency rectification in a potentially low-cost technology allow us to advance towards implementation of HF RFID applications in organic electronics. However, further work is needed to fully meet the complexity and performance which are required by such applications. Circuit techniques can be employed to improve the overall performance of the demodulator. In addition, a high-frequency model is needed to further facilitate the analysis and design phase.

Acknowledgments

This work was funded in the frame of the European FP7 project COSMIC (Grant agreement No. 247681).

References

[1] E. Cantatore, T.C.T. Geuns, G.H. Gelinck, E. van Veenendaal, A. Gruijthuijsen, L. Schrijnemakers, S. Drews, D.M. de Leeuw, A 13.56 MHz RFID system based on organic transponders, IEEE J. Solid-State Circ. 42 (2007) 84–92.

[2] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A.K. Tripathi, G.H. Gelink, J. Genoe, W. Dehaene, P. Heremans, Organic RFID transponder chip with data rate compatible with electronic product coding, Org. Electron. 11 (2010) 1176–1179.

[3] T. Sekitani, T. Someya, Stretchable organic integrated circuits for large-area electronic skin surfaces, MRS Bull. 37 (2012) 236–245.

[4] Y. Kato, S. Iba, T Sekitani, Y. Noguchi, K. Hizu, X. Wang, K. Takenoshita, Y. Takamatsu, S. Nakano, K. Fukuda, K. Nakamura, T. Yamaue, M. Doi, K. Asaka, H. Kawaguchi, M. Takamiya, T. Sakurai, T. Someya, A flexible lightweight Braille sheet display with plastic

actuators driven by an organic field-effect transistor active matrix, Int. Electron Dev. Meet. Technol. Dig. (2005) 105–108.
[5] H. Marien, M. Steyaert, E. van Veenendaal, P. Heremans, Analog techniques for reliable organic circuit design on foil applied to an 18 dB single-stage differential amplifier, Org. Electron. 11 (2010) 1357–1362.
[6] S. De Vusser, J. Genoe, P. Heremans, Influence of transistor parameters on the noise margin of organic digital circuits, IEEE Trans. Electron Dev. ED-53 (2006) 601–610.
[7] K. Myny, M.J. Beenhakkers, N.A.J.M. van Aerle, G.H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, Unipolar organic transistor circuits made robust by dual-gate technology, IEEE J. Solid-State Circ. 46 (2011) 1223–1230.
[8] K. Ishida, N. Masunaga, Z. Zhou, T. Yasufuku, T. Sekitani, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, T. Sakurai, A stretchable EMI measurement sheet with 8×8 coil array, 2 V organic CMOS decoder, and 70 dBm EMI detection circuits in 0.18 m CMOS, IEEE Int. Solid-State Circ. Conf. Dig. Technol. Pap. (2009) 472–473.
[9] R. Blache, J. Krumm, W. Fix, Organic CMOS circuits for RFID applications, IEEE Int. Solid-State Circ. Conf. Dig. Technol. Pap. (2009) 208–209.
[10] A. Knobloch, A. Manuelli, A. Bernds, W. Clemens, Fully printed integrated circuits from solution processable polymers, J. Appl. Phys. 96 (2004) 2286–2291.
[11] T. Someya, T. Sekitani, M. Takamiya, T. Sakurai, U. Zschieschang, H. Klauk, Printed organic transistors: toward ambient electronics, Int. Electron Dev. Meet. (2009) 1–6.
[12] M. Bohm, A. Ullmann, D. Zipperer, A. Knobloch, W.H. Glauert, W. Fix, Printable electronics for polymer RFID applications, IEEE Int. Solid-State Circ. Conf. Dig. Technol. Pap. (2006) 1034–1035.
[13] A. Daami, C. Bory, M. Benwadih, S. Jacob, R. Gwoziecki, I. Chartier, R. Coppard, C. Serbutoviez, L. Maddiona, E. Fontana, A. Scuderi, Fully printed organic CMOS technology on plastic substrates for digital and analog applications, IEEE Int. Solid-State Circ. Conf. Dig. Technol. Pap. (2011) 328–329.
[14] M. Guerin, A. Daami, S. Jacob, E. Bergeret, E. Benevent, P. Pannier, R. Coppard, High-gain fully-printed organic complementary circuits on flexible plastic foils, IEEE Trans. Electron Dev. 58 (2011) 3587–3593.
[15] P.F. Baude, D.A. Ender, M.A. Hasse, T.W. Kelley, D.V. Muyres, S.D. Theiss, Pentacene-based radio-frequency identification circuitry, Appl. Phys. Lett. 82 (2003) 3964–3966.
[16] S. Steudel, K. Myny, V. Arkhipov, C. Deibel, S. de Vusser, J. Genoe, P. Heremans, 50 MHz rectifier based on an organic diode, Nat. Mater. 4 (2005) 597–600.
[17] K. Myny, S. Steudel, P. Vicca, J. Genoe, P. Heremans, An integrated double half-wave organic Schottky diode rectifier on foil operating at 13.56 MHz, Appl. Phys. Lett. 93 (2008) 093305.
[18] F. Torricelli, E. Cantatore, A. Valleta, S. Jacob, M. Benwadih, M. Coppard, G. Fortunato, M. Rapisadra, L. Mariucci, Physically-based compact model of staggered p- and n-type organic thin-film transistors, in: Proc. of Int. Thin-Film Transistor Conf. 2012, pp. 116.
[19] F. Torricelli, Zs.M. Kovács-Vajna, L. Colalongo, A charge control analytical model for organic thin film transistors, Appl. Phys. Lett. 92 (2008) 113306.
[20] F. Torricelli, Z.M. Kovács-Vajna, L. Colalongo, A charge-based OTFT model for circuit simulation, IEEE Trans. Electron Dev. 56 (2009) 20–30.
[21] F. Torricelli, K. O'Neill, G.H. Gelinck, K. Myny, J. Genoe, E. Cantatore, Charge transport in organic transistors accounting for a wide distribution of carrier energies—Part II: TFT modeling, IEEE Trans. Electron Dev. 59 (2012) 1520–1528.
[22] O. Marinov, M.J. Deen, U. Zschieschang, H. Klauk, Organic thin-film transistors: Part I-compact DC modeling, Trans. Electron Dev. 56 (2009) 2952–2961.
[23] M. Rapisarda, A. Valletta, A. Daami, S. Jacob, M. Benwadih, R. Coppard, G. Fortunato, L. Mariucci, Analysis of contact effects in fully printed p-channel organic thin film transistors, Org. Electron. 13 (2012) 2017–2027.
[24] L. Mariucci, M. Rapisarda, A. Valletta, S. Jacob, M. Benwadih, G. Fortunato, Current spreading effects in fully printed p-channel organic thin film transistors with Schottky source-drain contacts, Org. Electron. 14 (2013) 86–93.
[25] A. Valletta, A. Daami, M. Benwadih, R. Coppard, G. Fortunato, M. Rapisarda, F. Torricelli, L. Mariucci, Contact effects in high performance fully printed p-channel organic thin film transistors, Appl. Phys. Lett. 99 (2011) 233309.
[26] S. Jacob, M. Benwadih, J. Bablet, I. Chartier, R. Gwoziecki, S. Abdinia, E. Cantatore, L. Maddiona, F. Tramontana, G. Maiellaro, L. Mariucci, G. Palmisano, R. Coppard, High performance printed n and p-type OTFTs for complementary circuits on plastic substrate, in: Proc. of the European solid-state device research conference 2012, pp. 173–176.
[27] S. Abdinia, M. Benwadih, E. Cantatore, I. Chartier, S. Jacob, L. Maddiona, G. Maiellaro, L. Mariucci, G. Palmisano, M. Rapisarda, F. Tramontana, A.H.M. van Roermund, Design of analog and digital building blocks in a fully printed complementary organic technology, in: Proc. of the European Solid-State Circuits Conf. 2012, pp. 145–148.
[28] G. Maiellaro, E. Ragonese, A. Castorina, S. Jacob, M. Benwadih, R. Coppard, E. Cantatore, G. Palmisano, High-gain operational transconductance amplifiers in a printed complementary organic TFT technology on flexible foil, IEEE Trans. Circ. Syst. I (2013). in press.
[29] K. Myny, M. Rockele, A. Chasin, D.V. Pham, J. Steiger, S. Botnaras, D. Weber, B. Herold, J. Ficker, B. van der Putten, G. Gelinck, J. Genoe, W. Dehaene, P. Heremans, Bidirectional communication in an HF hybrid organic/solution-processed metal-oxide RFID tag, IEEE Int. Solid-State Circ. Conf. Dig. Technol. Pap. (2012) 312–313.