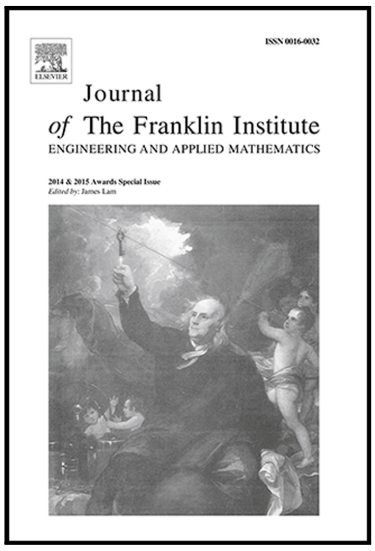

Suppressionof DC-Link Voltage Unbalance in Three-Level Neutral-Point Clamped Converters

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PII: S0016-0032(17)30629-4
DOI: 10.1016/j.jfranklin.2017.11.039
Reference: FI 3249

To appear in: *Journal of the Franklin Institute*

Received date: 22 April 2016
Revised date: 25 October 2017
Accepted date: 27 November 2017

Please cite this article as: Mario Porru , Alessandro Serpi , Ignazio Marongiu , Alfonso Damiano , Suppressionof DC-Link Voltage Unbalance in Three-Level Neutral-Point Clamped Converters, *Journal of the Franklin Institute* (2017), doi: 10.1016/j.jfranklin.2017.11.039

Highlights

- Two control approaches for DC-Link equalization of a three-level NPC are proposed
- The Digital Scalar PWM is extended to a three-level NPC
- The proposed control schemes are compared to the multilevel space vector PWM
- DC-Link equalization is achieved successfully at any power factor
- P-based NPC control minimizes voltage and current ripple on DC-Link *capacitors*

Suppression of DC-Link Voltage Unbalance in Three-Level Neutral-Point Clamped Converters

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Abstract

Two different control approaches for suppressing DC-link voltage unbalance in Three-Level Neutral-Point Clamped Converters (NPCs) are presented in this paper. They both guarantee DC-link voltage equalization over any NPC operating conditions, i.e. when the NPC feeds or is supplied by the main AC grid at different active and/or reactive power rates. The proposed control approaches consist of either a hysteresis or a proportional regulator, each of which synthesizes the most suitable control action based on the actual DC-link voltage unbalance. Particularly, two different PWM techniques have been developed in order to achieve DC-link voltage equalization successfully, preserving NPC voltage and current waveforms at the same time. The performances achievable by means of both the proposed control approaches have been compared to each other through an extensive simulation study in order to highlight their most important advantages and drawbacks, as well as their effectiveness over any operating conditions. Particularly, both control approaches are validated in the Matlab-Simulink environment referring to DC-link voltage equalization of an NPC that represents the point of common coupling between a DC microgrid and the main AC grid.

Keywords: Multilevel converter, Three-level converter, Neutral-point-clamped converter, Pulse width modulation, Digital Scalar PWM, Space Vector PWM, DC-link voltage equalization, Simulations

1. Introduction

The three-level Neutral-Point Clamped Converter (NPC) is widely used in industrial applications [1]–[3]. This is mainly due to several advantages compared to conventional two-level converters, among which lower losses, higher switching frequency, reduced filter size and weight, improved reliability and lower costs [4]. These advantages guarantee high performances in a wide range of applications, such as renewable energy sources [5], [6], hybrid energy storage systems [7]–[10], automotive [10]–[12] and power system management [13]–[15]. Apart from these advantages, NPC is characterized by a relatively complex topology, i.e. four switches per leg and two DC-link capacitors. However, the increased degrees of freedom compared to conventional two-level converters enable appropriate Pulse Width Modulation (PWM) techniques, which can be developed in order to increase overall system performances [16], [17]. In particular, apart from guaranteeing appropriate reference AC phase and/or chain voltages, most of these techniques are able to satisfy further requirements, such as DC-link voltage equalization [13], [18], capacitor current and/or voltage ripple reduction [19], [20], Total Harmonic Distortion (THD) and/or switching losses minimization [21], [22].

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Among the various PWM approaches for multilevel converters proposed in the literature, multilevel carrier-based PWM, selective harmonic elimination and space vector PWM are surely the most popular [23]. Multilevel carrier-based PWM generally employs several triangle carriers, which are compared to one reference signal in order to synthesize the command signals of each switch of a converter leg [23]–[28]. Among these, Sinusoidal PWM (SPWM), which employs sinusoidal reference signals, is largely employed in industrial applications. However, either Third Harmonic injection PWM (THPWM) and space vector PWM (SV-PWM) can be alternatively used, both of which enable an increased DC-link voltage exploitation. Another carrier-based multilevel PWM technique is the Sub-Harmonic PWM (SH-PWM) [29], which requires few contiguous carriers in order to determine all the switching signals. Switching Frequency Optimal PWM (SFO-PWM) [30] is similar to SH-PWM, but a zero-sequence voltage is added to the reference signal in order to act as an SV-PWM [31], [32], thus leading to an increased DC-link voltage exploitation compared to SH-PWM. In this context, it is worth noting that both SH-PWM and SFO-PWM exploit upper and lower switches more than intermediate switches; this drawback can be overcome by increasing the frequency of intermediate carriers compared to upper and lower carriers. A major issue of multilevel carrier-based PWM occurs when the modulation index and, thus, the amplitude of the reference signal is low. In this case, many switches become idle, thus the multilevel converter operates with a reduced number of levels. This issue can be addressed by exploiting switching state redundancy appropriately; specifically, the reference signal can be vertically-shifted from one cycle to the next in order to cross different carriers in different cycles. As a result, all the converter levels can be used alternatively over a number of cycles, thus the carrier frequency can be increased by only slightly increasing the total switching losses [23].

The selective harmonic elimination method, also called fundamental switching frequency method, is based on the theory proposed in [33], [34]. It consists of selecting the conducting angles of each converter leg in order to achieve the reference magnitude of the fundamental voltage component, while suppressing the highest number of low-order harmonic components. Consequently, reduced filter size and switching losses are achieved by using few commutations per cycle [35]–[37]. However, as far as low modulation indexes are concerned, the fundamental switching frequency method can only be employed with difficulty. Hence, it can be combined with unipolar programmed PWM, leading to a generalized selective harmonic modulation method called virtual stage PWM [23]. Further selective harmonic elimination PWMs have been proposed in the literature with the aim of improving output voltage waveforms and/or reducing computational effort in solving transcendental equations [36]–[38]. In particular, transcendental equations are generally solved by means of iterative methods (Newton-Raphson). Nevertheless, genetic algorithms and resultant theory can be considered [39]–[41]. In particular, appropriate initial conditions are needed for the Newton-Raphson method, but achievement of the solution is not guaranteed. Better results can be achieved by the Resultant method, which converts transcendental equations into polynomial equations. However, polynomial degrees increase with the number of levels, leading to high computational costs.

Multilevel Space Vector Modulation (MSVM) is an extended version of the two-level Space Vector Modulation (SVM) for multilevel converters [42]–[46]. In particular, SPWM consists of achieving the reference space vector as a weighted sum of the two nearest “base” vectors and the zero-voltage vectors. Whereas MSVM generally computes the reference voltage vector as a weighted sum of the three nearest “base” vectors in order to minimize the harmonic content of the output voltage [47]. Alternatively, other MSVM approaches could be followed at the cost of increased complexity. One attractive feature of MSVM consists of exploiting switching state redundancy for DC-link voltage equalization purposes [48]. However, the selection of the most appropriate redundant states is quite complex, their use leading also to additional switching losses

[23]. Consequently, optimal switching sequences should be considered, as in [49].

Regarding DC-link voltage equalization, non ideal components and inappropriate exploitation of redundant switching states may lead to unbalanced power exchanges between high-side and low-side capacitors. This causes unsuitable neutral-point voltage drifts, which must be suppressed in order to avoid output voltage errors and ripple, voltage stresses on power semiconductor devices and equipment damages [50]. Although neutral-point voltage drifts may be addressed by natural balancing [51], DC-link voltage equalization generally relies on appropriate PWM techniques. However, some of these are unusable with high modulation indexes and low power factors and they may increase the THD of line currents as well [25], [43], [52].

In this context, two different control approaches are presented in this paper, which enable suitable DC-link voltage equalization by preserving NPC performances at the same time. The first approach (Hysteresis NPC control) consists of employing a hysteresis regulator fed by the DC-link voltage unbalance, jointly with a suitable PWM pattern (HML-PWM). Such a simple solution can be easily implemented, but it is characterized by unsuitable current ripple through DC-link capacitors at steady state operation. Whereas the second approach (P-based NPC control) employs a proportional regulator combined with another PWM pattern (PS-PWM). As a result, it enables a smoother regulation of DC-link voltages than the previous one, reducing capacitor current and voltage ripple at the same time. It is worth noting that HML-PWM and PS-PWM are both extended versions of the Digital Scalar PWM for the NPC. The Digital Scalar PMW has been employed successfully in two-level converters due to its simple implementation [53], [54]. Consequently, one of the contributions of the paper consists in the extension and performance assessment of Digital Scalar PWM for three-level converters. The proposed control approaches are both validated through an extensive simulation study, which has been carried out in the Matlab-Simulink environment in order to assess their effectiveness in any operating conditions, i.e. at different active and/or reactive power rates. In particular, the simulation study refers to the DC-link voltage equalization of an NPC that represents the Point of Common Coupling (PCC) between a DC microgrid and the main AC grid. Simulations regard also the comparison between Hysteresis and P-based NPC controls with the well-known MSVM in order to highlight the most important advantages and drawbacks.

The paper is structured as follows: NPC modeling and fundamentals of DC-link voltage control are both resumed briefly in Section 2, while the proposed Hysteresis and P-based NPC controls are described in detail in Section 3 and 4 respectively. Simulation results are shown and discussed extensively in Section 5, while concluding remarks are given in Section 6. All the symbols employed in the paper are summed up in the Appendix, together with their corresponding meaning.

2. NPC Mathematical Modeling

2.1. Basic equations

Referring to the schematic representation of a three-phase NPC shown in Fig. 1, it can be seen that each leg consists of four switches and two clamping diodes. The DC-link voltage is shared between the high-side and low-side capacitors, whose voltages are denoted by V_H and V_L respectively, their capacitances being assumed equal to each other. Hence, denoting by V_x the voltage across the generic phase terminal x and the neutral point N, three different leg states can be defined: H, L and M. These depend on the switching states as pointed out in Table 1. Consequently, the per unit phase terminal voltages can be defined as

$$v_x = \delta_H v_H - \delta_L v_L \quad , \quad x \in \{a,b,c\} \; , \delta \in \{\alpha,\beta,\gamma\} \tag{1}$$

where δ_H and δ_L denote the duty cycles of the H and L states of the leg x, $\{\alpha,\beta,\gamma\}$ being the duty

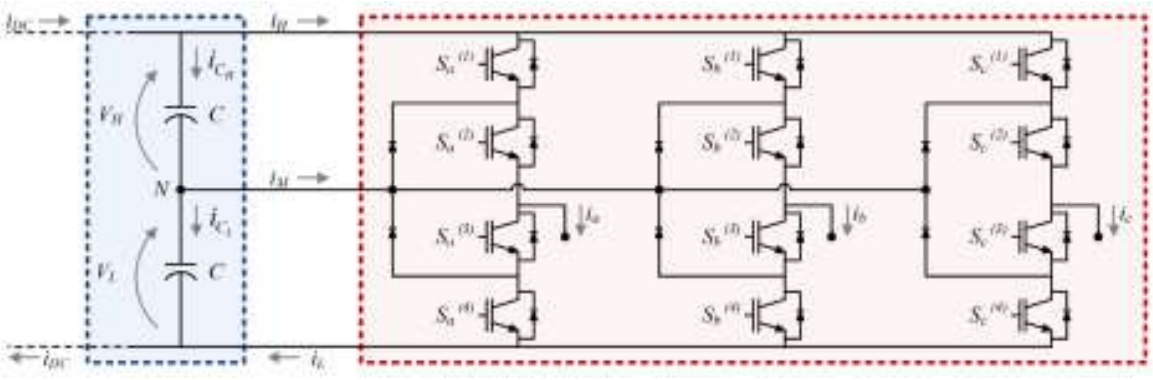

Fig. 1. A three-phase NPC (red box) and its DC-link (blue box).

Table 1
Switching and Leg States.

Leg State	*Switching States*				V_x
	$S_x^{(1)}$	$S_x^{(2)}$	$S_x^{(3)}$	$S_x^{(4)}$	
H	1	1	0	0	V_H
M	0	1	1	0	0
L	0	0	1	1	$-V_L$

cycles of the legs $\{a,b,c\}$ respectively. Furthermore, v_H and v_L are the per unit capacitor voltages, which are defined as

$$v_H = \frac{V_H}{V_H + V_L} \quad , \quad v_L = \frac{V_L}{V_H + V_L} \quad . \tag{2}$$

Still referring to (1), the duty cycles of each leg must satisfy the following equation:

$$\delta_H + \delta_M + \delta_L = 1 \quad , \quad \delta \in \{\alpha, \beta, \gamma\} \quad . \tag{3}$$

Consequently, based on both (1) and (3), the generic per unit phase terminal voltage v_x is bounded in accordance with

$$-v_L \le v_x \le v_H \quad , \quad x \in \{a,b,c\} \quad . \tag{4}$$

Considering now the per unit chain voltages, they can be expressed as

$$v_{ab} = v_a - v_b \, , \quad v_{bc} = v_b - v_c \, , \quad v_{ca} = v_c - v_a \quad . \tag{5}$$

Finally, DC-link current relationships are

$$i_H = \alpha_H \, i_a + \beta_H \, i_b + \gamma_H \, i_c \, , \quad i_L = -\left(\alpha_L \, i_a + \beta_L \, i_b + \gamma_L \, i_c\right) \tag{6}$$

where i_a, i_b and i_c denote the phase currents.

2.2. DC-Link Voltage Control

In order to define a control strategy for equalizing the DC-link voltages, reference can be made to Fig. 1 again, based on which, the time derivative of both V_H and V_L can be expressed as

$$\frac{dV_H}{dt} = \frac{i_{DC} - i_H}{C} \, , \quad \frac{dV_L}{dt} = \frac{i_{DC} - i_L}{C} \tag{7}$$

in which i_{DC} denotes the DC current and C is the capacitance of each DC-link capacitor. As a consequence, subtracting (7) from each other yields

$$\frac{dV_M}{dt} = \frac{i_M}{C} \tag{8}$$

where V_M and i_M are the DC-link voltage and current unbalance respectively, which are defined as

$$V_M = V_H - V_L \ , \quad i_M = -\left(i_H - i_L\right). \tag{9}$$

Therefore, (8) suggests that DC-link voltage unbalance can be managed by means of i_M. Thus, either a hysteresis or a proportional regulator can be employed in order to suppress DC-link voltage unbalance through appropriate PWM patterns [55]–[57]. In particular, the first solution is simple and easy to be implemented but it leads to unsuitable current and voltage ripple on DC-link capacitors [56]. Whereas the second approach enables an appropriate i_M management but requires an increased level of complexity [57]. It is worth noting that these solutions need different PWM techniques, whose development requires the definition of voltage sectors (σ_v) in accordance with the binary signs of the reference chain voltages $\{s_{ab}^*, s_{bc}^*, s_{ca}^*\}$, as summed up in Table 2. Consequently, a new set of indexes $\{u,v,w\}$ can be introduced, each of which alternatively denotes one of the phase terminals $\{a,b,c\}$ over each voltage sector in accordance with Table 3. As a result, it is possible to state that v_{uv} always represents the voltage of maximum magnitude, v_{vw} and v_{wu} being always opposite to v_{uv}:

$$\left|v_{uv}\right| \geq \left|v_{vw}\right| \ , \quad \left|v_{uv}\right| \geq \left|v_{wu}\right| \ , \quad s_{uv} = \overline{s}_{vw} = \overline{s}_{wu} \ . \tag{10}$$

Consequently, (1) and (4) become respectively

$$v_x = \delta_H v_H - \delta_L v_L \quad , \quad x \in \{u,v,w\} \ , \ \delta \in \{\varphi,\psi,\xi\} \tag{11}$$

$$-v_L \leq v_x \leq v_H \quad , \quad x \in \{u,v,w\} \tag{12}$$

where $\{\varphi,\psi,\xi\}$ denote the duty cycles of the legs $\{u,v,w\}$. Furthermore, (3) can now be expressed as

$$\delta_H + \delta_M + \delta_L = 1 \quad , \quad \delta \in \{\varphi,\psi,\xi\} \ . \tag{13}$$

Finally, based on (11), (5) and (6) become

$$\begin{aligned} v_{uv} &= \left(\varphi_H - \psi_H\right)v_H - \left(\varphi_L - \psi_L\right)v_L \\ v_{vw} &= \left(\psi_H - \xi_H\right)v_H - \left(\psi_L - \xi_L\right)v_L, \quad v_{wu} = \left(\xi_H - \varphi_H\right)v_H - \left(\xi_L - \varphi_L\right)v_L \end{aligned} \tag{14}$$

$$i_H = \varphi_H i_u + \psi_H i_v + \xi_H i_w \ , \quad i_L = -\left(\varphi_L i_u + \psi_L i_v + \xi_L i_w\right). \tag{15}$$

As a result, based on (8) and (15), the following equation is achieved:

$$\frac{dx}{dt} = Bu \ , \ x = V_M \ , \ B = \frac{1}{C}\left[-i_u \quad i_u \quad -i_v \quad i_v \quad -i_z \quad i_z\right], u = \left[\varphi_H \quad \varphi_L \quad \psi_H \quad \psi_L \quad \xi_H \quad \xi_L\right]^T \tag{16}$$

the corresponding equivalent block scheme being depicted in Fig. 2. Considering both (14) and (15), it can be noticed that different combinations of $\{\varphi,\psi,\xi\}$ may lead to the same chain voltages but to different DC-link currents. Therefore, actual current sectors (σ_i) can be defined in

Table 2
Voltage Sectors

s_{ab}	0	0	1	1	1	0
s_{bc}	1	0	0	0	1	1
s_{ca}	1	1	1	0	0	0
σ_v	I	II	III	IV	V	VI

Table 3
Phase Terminal Indexes

σ_v	I	II	III	IV	V	VI
U	a	c	b	a	c	b
V	b	a	c	b	a	c
W	c	b	a	c	b	a

Table 4
Current Sectors

s_u	0	0	1	1	1	0
s_v	1	0	0	0	1	1
s_w	1	1	1	0	0	0
σ_i	I	II	III	IV	V	VI

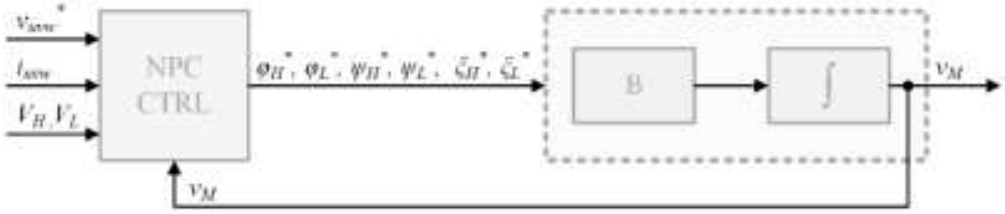

Fig. 2. Equivalent block scheme of the NPC.

accordance with the binary signs of the actual phase currents $\{s_u,s_v,s_w\}$, as pointed out in Table 4. Consequently, the knowledge of both σ_v and σ_i can be suitably exploited in order to equalize DC-link voltages as needed, for any given reference chain voltages.

3. Hysteresis NPC control

The hysteresis NPC control consists of selecting the duty cycles of the NPC legs in accordance with a binary signal ε. This is synthesized from DC-link voltage unbalance through an appropriate two-level hysteresis regulator, as shown in Fig. 3. In particular, ε is high when high-side capacitor needs to be charged; otherwise, ε is low. Furthermore, the knowledge of actual NPC phase currents is also needed in order to carry out the required charging/discharging task. Similarly, the reference chain voltages must be considered, whose achievement is mandatory in order to preserve appropriate AC voltage and current waveforms. Based on all this information, a suitable PWM technique (HML-PWM) can be developed for achieving DC-link voltage equalization successfully, as detailed in the following subsection.

3.1. HML-PWM

HML-PWM has been developed starting from the knowledge of the voltage sector (σ_v); considering only odd voltage sectors (I, III, V) at first, v_{uv} is always positive in accordance with (10). Consequently, based on (14), both φ_L and ψ_H are always imposed equal to zero because these duty cycles do not contribute to the achievement of a positive v_{uv} value. As a result, (14) becomes

$$v_{uv}^{*}=\varphi_H v_H+\psi_L v_L\ ,\quad v_{vw}^{*}=-\psi_L v_L-\left(\xi_H v_H-\xi_L v_L\right),\quad v_{wu}^{*}=-\varphi_H v_H+\left(\xi_H v_H-\xi_L v_L\right)\ . \tag{17}$$

Whereas high-side and low-side DC-link currents can be determined from (15) as

$$i_H=\varphi_H\cdot i_u+\xi_H\cdot i_w\ ,\quad i_L=-\left(\psi_L\cdot i_v+\xi_L\cdot i_w\right)\ . \tag{18}$$

Similar considerations can be made also for even voltage sectors (II, IV, VI), in correspondence to which v_{uv} is always negative. Consequently, both φ_H and ψ_L are always set to zero, thus (14) and (15) become respectively

$$v_{uv}^{*}=-\varphi_L v_L-\psi_H v_H\ ,\quad v_{vw}^{*}=\psi_H v_H-\left(\xi_H v_H-\xi_L v_L\right),\quad v_{wu}^{*}=\varphi_L v_L+\left(\xi_H v_H-\xi_L v_L\right) \tag{19}$$

$$i_H=\psi_H\cdot i_v+\xi_H\cdot i_w\ ,\quad i_L=-\left(\varphi_L\cdot i_u+\xi_L\cdot i_w\right). \tag{20}$$

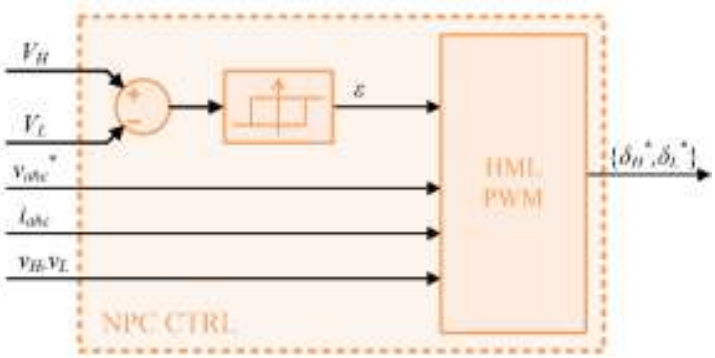

Fig. 3. Equivalent block control scheme of the proposed Hysteresis NPC control.

Therefore, different choices of all the remaining duty cycles have to be performed depending on the output signal of the hysteresis regulator (ε). If ε is high, i_H has to be minimized in order to recharge or discharge less the high-side capacitor to the maximum extent. Otherwise, if ε is low, i_H has to be maximized. Apart from σ_v, this goal requires the knowledge of the signs of actual phase currents, as easily detectable from both (18) and (20). Therefore, actual current sectors (σ_i) must be considered as well.

Hence, based on the previous considerations, three different PWM patterns can be determined: H-PWM, M-PWM and L-PWM. These are characterized by different duty cycles for a given reference chain voltage vector, as pointed out in Table 5. H-PWM consists of maximizing φ_H or ψ_H over odd or even voltage sectors respectively. Similarly, L-PWM enables ψ_L or φ_L maximization, whereas M-PWM allows both ξ_H and ξ_L minimization. Among these PWM patterns, the most suitable one should be chosen based on $\{\varepsilon,\sigma_v,\sigma_i\}$ in order to suppress DC-link voltage unbalance, as pointed out in Table 6.

In conclusion, the overall scheme of the proposed HML-PWM is depicted in Fig. 4. It is worth noting that all the PWM patterns guarantee the achievement of the reference chain voltages, thus prioritizing power flow management compared to DC-link voltage equalization needs.

Table 5
H-PWM, M-PWM and L-PWM patterns

	H-PWM	*M-PWM*	*L-PWM*
φ_H	$max\left\{0,min\left\{\frac{v_{uv}^*}{v_H},1\right\}\right\}$	$max\left\{0,min\left\{-\frac{v_{wu}^*}{v_H}+\xi_H,1\right\}\right\}$	$max\left\{0,\frac{v_{uv}^*-v_L}{v_H}\right\}$
φ_L	$max\left\{0,-\frac{v_{uv}^*+v_H}{v_L}\right\}$	$max\left\{0,min\left\{\frac{v_{wu}^*}{v_L}+\xi_L,1\right\}\right\}$	$max\left\{0,min\left\{-\frac{v_{uv}^*}{v_L},1\right\}\right\}$
ψ_H	$max\left\{0,min\left\{-\frac{v_{uv}^*}{v_H},1\right\}\right\}$	$max\left\{0,min\left\{\frac{v_{vw}^*}{v_H}+\xi_H,1\right\}\right\}$	$max\left\{0,-\frac{v_{uv}^*+v_L}{v_H}\right\}$
ψ_L	$max\left\{0,-\frac{v_{uv}^*-v_H}{v_L}\right\}$	$max\left\{0,min\left\{-\frac{v_{vw}^*}{v_L}+\xi_L,1\right\}\right\}$	$max\left\{0,min\left\{\frac{v_{uv}^*}{v_L},1\right\}\right\}$
ξ_H	$max\left\{0,min\left\{-\frac{v_{vw}^*}{v_H}+\psi_H,\frac{v_{wu}^*}{v_H}+\varphi_H\right\}\right\}$	$max\left\{0,-\frac{v_{vw}^*+v_L}{v_H},\frac{v_{wu}^*-v_L}{v_H}\right\}$	$max\left\{0,-\frac{v_{vw}^*+v_L}{v_H},\frac{v_{wu}^*-v_L}{v_H}\right\}$
ξ_L	$max\left\{0,\frac{v_{vw}^*-v_H}{v_L},-\frac{v_{wu}^*+v_H}{v_L}\right\}$	$max\left\{0,\frac{v_{vw}^*-v_H}{v_L},-\frac{v_{wu}^*+v_H}{v_L}\right\}$	$max\left\{0,min\left\{\frac{v_{vw}^*}{v_L}+\psi_L,-\frac{v_{wu}^*}{v_L}+\varphi_L\right\}\right\}$

Table 6
Look-up Table of HML-PWM implementation

ε	σ_i \ σ_v	*I, III, V*	*II, IV, VI*	ε	σ_i \ σ_v	*I, III, V*	*II, IV, VI*
0	*I, VI*	H-PWM	L-PWM	1	*I, VI*	L-PWM	H-PWM
	II	M-PWM	M-PWM		*II*	H-PWM	H-PWM
	III, IV	L-PWM	H-PWM		*III, IV*	H-PWM	L-PWM
	V	H-PWM	H-PWM		*V*	M-PWM	M-PWM

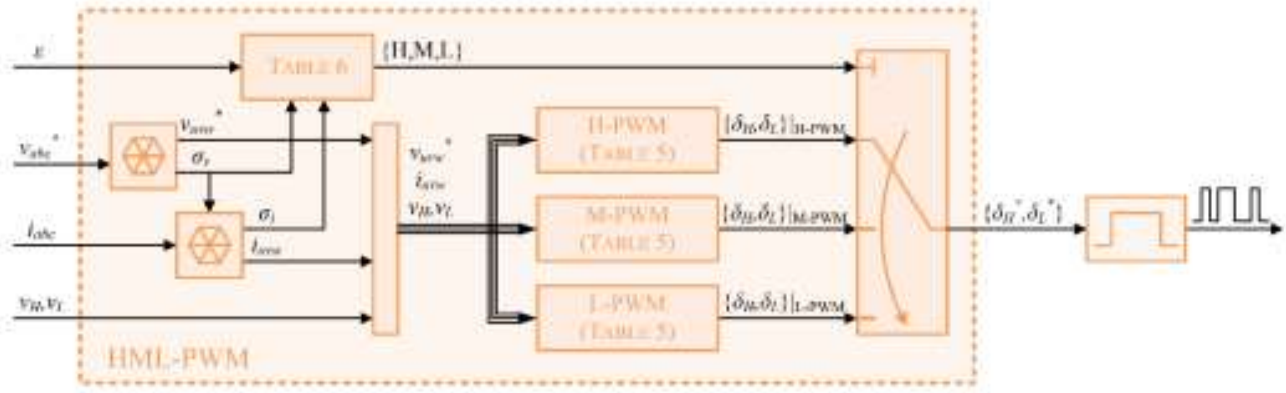

Fig. 4. Overall control scheme of the proposed HML-PMW.

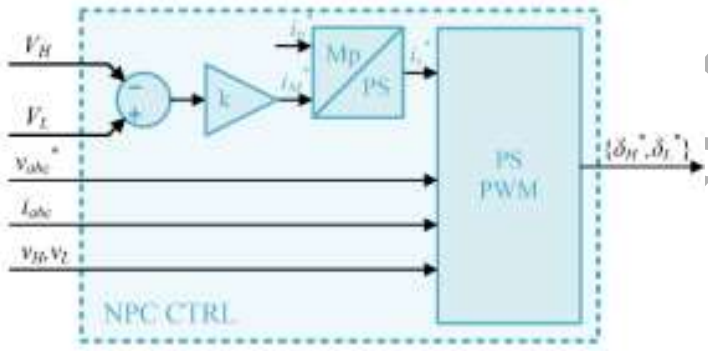

Fig. 5. Equivalent block control scheme of the proposed P-based NPC control.

4. P-based NPC control

The P-based NPC control has been developed with the aim of improving the performances of the hysteresis NPC control described in the previous section. A smooth regulation of DC-link voltages can be assured by means of DC-link currents, which should be driven appropriately in order to avoid their maximization or minimization when unnecessary.

Hence, referring to (11), it can be assumed that the H and L states of each leg cannot occur over the same sampling time interval. Consequently, δ_H and δ_L are equal to zero alternatively:

$$\delta_H \cdot \delta_L = 0 \quad , \quad \delta \in \{x,y,z\} . \tag{21}$$

It is worth noting that such an assumption does not affect the phase terminal voltages, which are still bounded in accordance with (12). Thus, based on both (11) and (21), the following relationships can be introduced:

$$\delta_H = \frac{|v_x| + v_x}{2v_H} , \; \delta_L = \frac{|v_x| - v_x}{2v_L} \quad , \quad x \in \{u,v,w\} \; , \; \delta \in \{\varphi,\psi,\xi\} . \tag{22}$$

Consequently, by substituting (22) in (15), i_H and i_L can be further expressed as:

$$i_H = \frac{1}{2v_H}\left(\sum_x |v_x| i_x + \sum_x v_x i_x\right) \; , \quad i_L = -\frac{1}{2v_L}\left(\sum_x |v_x| i_x - \sum_x v_x i_x\right) \; , \quad x \in \{u,v,w\} \; . \tag{23}$$

Based on (23), it is possible to introduce two additional DC-link currents, i.e. i_p and i_s, which are defined respectively as

$$i_p = v_H i_H + v_L i_L = \sum_x v_x i_x \; , \quad i_s = v_H i_H - v_L i_L = \sum_x |v_x| i_x \; , \quad x \in \{u,v,w\} \; . \tag{24}$$

In particular, i_p represents the equivalent power current, which is proportional to the NPC active power. Whereas i_s is an auxiliary current that depends on both i_p and i_M as

$$i_s = \left(v_H - v_L\right)\cdot i_p + \left(2v_H v_L\right)\cdot i_M \quad . \tag{25}$$

Consequently, i_s can be set in accordance with DC-link voltage equalization needs, without affecting the power exchange between the DC microgrid and the main AC grid. A suitable i_M^* can be synthesized as

$$i_M^* = -k\cdot V_M \tag{26}$$

where k can be set in accordance with (8) in order to achieve appropriate dynamic performances. In particular, i_M^* can be assumed equal to i_M because it can be varied almost instantaneously, especially compared with DC-link voltage dynamic response. Therefore, the substitution of (26) in (8) leads to

$$\frac{dV_M}{dt} + \frac{k}{C}\cdot V_M = 0\ . \tag{27}$$

Hence, denoting the desired bandwidth of the DC-link voltage unbalance control loop by f_{DC}, k can be chosen in accordance with the following relationship:

$$\frac{k}{C} = 2\pi f_{DC} \qquad \rightarrow \qquad k = 2\pi f_{DC} C\ . \tag{28}$$

It is worth noting that k depends on both f_{DC} and C, namely fast DC-link voltage unbalance suppression and/or large C value lead to high k values in accordance with (28). It is also worthy of note that only a simple proportional regulator is needed because i_M^* should be zero when DC-link voltage unbalance does not occur. As a result, assuming i_p^* as the required power exchange, the reference i_s value can be computed easily from (25) as

$$i_s^* = \left(v_H - v_L\right)\cdot i_p^* + \left(2v_H v_L\right)\cdot i_M^* \quad . \tag{29}$$

The schematic representation of the P-based NPC control is shown in Fig. 5. It can be seen that, apart from i_s^*, further information is required. The knowledge of actual NPC phase currents and reference chain voltages is mandatory, as for hysteresis NPC control. In addition, in order to track i_s^* successfully, a suitable PWM technique has to be developed (PS-PWM), as detailed in the following subsection.

4.1. PS-PWM

Considering the per unit reference chain voltages in the uvw frame, they can be expressed as

$$v_{uv}^* = v_u - v_v\ ,\quad v_{vw}^* = v_v - v_w\ ,\quad v_{wu}^* = v_w - v_u\ . \tag{30}$$

Therefore, based on (30), v_u and v_v can be expressed as:

$$v_u = -v_{wu}^* + v_w\ ,\quad v_v = v_{vw}^* + v_w\ . \tag{31}$$

Thus, the substitution of (31) in (12) yields

$$v_{w,min} \le v_w \le v_{w,max} \tag{32}$$

where:

$$v_{w,min} = max\left\{v_{wu}^*, -v_{vw}^*\right\} - v_L\ ,\quad v_{w,max} = min\left\{v_{wu}^*, -v_{vw}^*\right\} + v_H\ . \tag{33}$$

As a result, it can be stated that the reference chain voltages can be successfully achieved for any v_w that complies with (32). Hence, by substituting (31) in (24), the following results are achieved:

$$i_p = -v_{wu}^* i_u + v_{vw}^* i_v + v_w\left(i_u + i_v + i_w\right) \tag{34}$$

$$i_s = \left|-v_{wu}^* + v_w\right|\cdot i_u + \left|v_{vw}^* + v_w\right|\cdot i_v + \left|v_w\right|\cdot i_w\quad . \tag{35}$$

Table 7
The i_s expression for odd and even voltage sectors

Odd Voltage Sectors		*Even Voltage Sectors*	
i_s	v_w *range*	i_s	v_w *range*
$v^*_{wu}\cdot i_u - v^*_{vw}\cdot i_v$	$v_{w,min} \le v_w \le v^*_{wu}$	$v^*_{wu}\cdot i_u - v^*_{vw}\cdot i_v$	$v_{w,min} \le v_w \le -v^*_{vw}$
$-v^*_{wu}\cdot i_u - v^*_{vw}\cdot i_v + 2\cdot v_w\cdot i_u$	$v^*_{wu} < v_w \le 0$	$v^*_{wu}\cdot i_u + v^*_{vw}\cdot i_v + 2\cdot v_w\cdot i_v$	$-v^*_{vw} < v_w \le 0$
$-v^*_{wu}\cdot i_u - v^*_{vw}\cdot i_v - 2\cdot v_w\cdot i_v$	$0 < v_w \le -v^*_{wu}$	$v^*_{wu}\cdot i_u - v^*_{vw}\cdot i_v - 2\cdot v_w\cdot i_u$	$0 < v_w \le v^*_{wu}$
$-v^*_{wu}\cdot i_u + v^*_{vw}\cdot i_v$	$-v^*_{wu} < v_w \le v_{w,max}$	$-v^*_{wu}\cdot i_u + v^*_{vw}\cdot i_v$	$v^*_{wu} < v_w \le v_{w,max}$

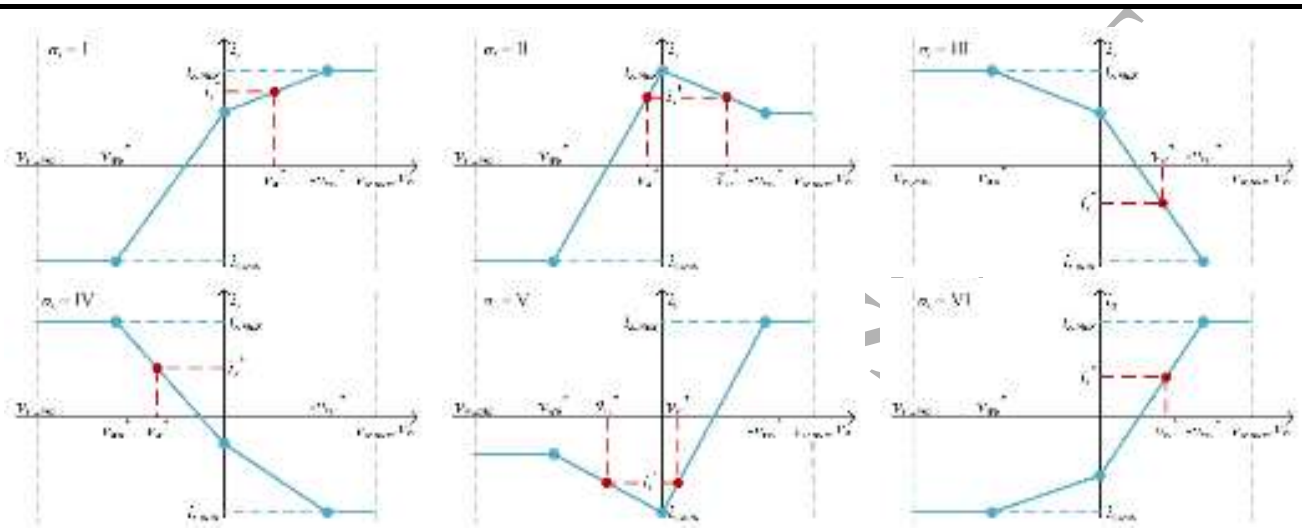

Fig. 6. The i_s evolution over any odd voltage sectors and any current sector.

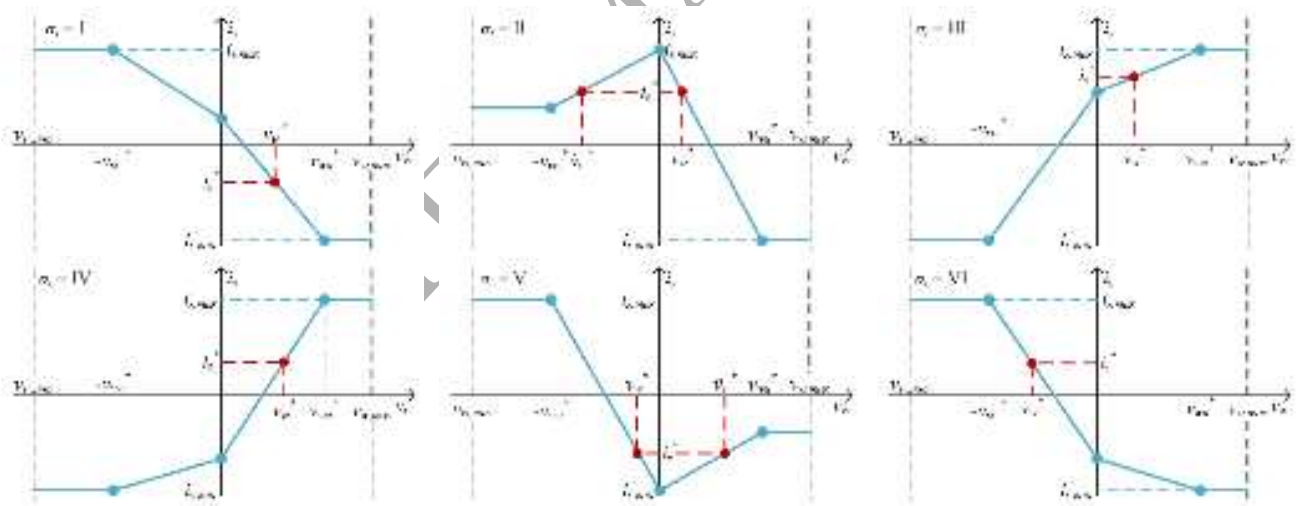

Fig. 7. The i_s evolution over any even voltage sector and any current sector.

Consequently, assuming the sum of the phase currents equal to zero, as occurs in isolated star-connected three-phase systems, it can be stated that i_p does not depend on v_w. Consequently, i_s can be controlled by v_w in accordance with DC-link voltage equalization needs, without affecting the power exchange between the DC microgrid and the main AC grid.

In order to perform an i_s control, reference can be made to (32) and (35). In this context, both voltage and current sectors must be considered, as for the HML-PWM. In particular, over odd and even voltage sectors, (33) becomes respectively

$$v_{w,min} = -v^*_{vw} - v_L \ , \quad v_{w,max} = v^*_{wu} + v_H \tag{36}$$

$$v_{w,min} = v_{wu} - v_L \ , \quad v_{w,max} = -v_{vw} + v_H \ . \tag{37}$$

As a consequence, based on either (36) or (37), the i_s evolution with v_w can be achieved for each (σ_v,σ_i) pair of values, as pointed out in Table 7 and highlighted in both Fig. 6 and Fig. 7. From these it can be seen that minimum and maximum values of i_s are generally achieved in correspondence with either $v_w^{(+)}$ or $v_w^{(-)}$, which are defined respectively as

$$v_w^{(+)} = max\left\{v_{wu}^*, -v_{vw}^*\right\} \quad , \qquad v_w^{(-)} = min\left\{v_{wu}^*, -v_{vw}^*\right\} \ . \tag{38}$$

Hence, if at least one of these values lies within $[v_{w,min},v_{w,max}]$, it means that a plateau region occurs, as highlighted in Fig. 6 and Fig. 7. Within these operating regions, any further variation of v_w does not affect i_s because the sum of the phase currents equals zero, as assumed previously. Still referring to both Fig. 6 and Fig. 7, it can be seen that minimum and maximum values of i_s occur when v_w is zero within both II and V current sectors. In these cases, a given i_s^* may correspond to two different v_w values: v_w^* and $\tilde{v}_w^*$. However, v_w^* should be chosen because it lies within the v_w interval that guarantees a linear control of i_s within its full range.

In conclusion, the overall control scheme of the PS-PWM is shown in Fig. 8. For any given reference chain voltages and i_s^*, the most suitable v_w^* can be chosen in accordance with Table 8. It is then possible to compute the other phase terminal voltages by means of (31) and thus, all the H and L duty cycles by means of (22).

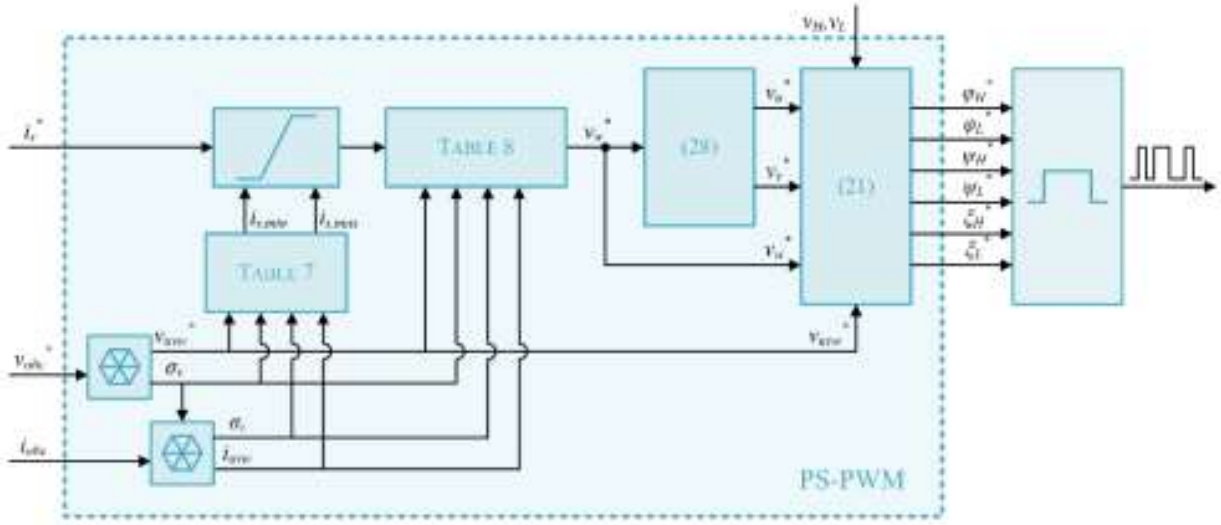

Fig. 8. Equivalent block control scheme of the proposed PS-PWM.

Table 8
The v_w^* expression for odd and even voltage sectors

σ_i	σ_v = I, III, V	σ_i	σ_v = II, IV, VI
I IV	$\frac{1}{2}max\left\{v_{wu}^* + \frac{i_s^* + v_{vw}^* i_v}{i_u}, -v_{vw}^* - \frac{i_s^* + v_{wu}^* i_u}{i_v}\right\}$	I IV	$\frac{1}{2}min\left\{v_{wu}^* - \frac{i_s^* - v_{vw}^* i_v}{i_u}, -v_{vw}^* + \frac{i_s^* - v_{wu}^* i_u}{i_v}\right\}$
II	$-\frac{1}{2}\left(v_{vw}^* + \frac{i_s^* + v_{wu}^* i_u}{i_v}\right)$ for $\sigma_0 = 0$	II	$-\frac{1}{2}\left(v_{wu}^* - \frac{i_s^* - v_{vw}^* i_v}{i_u}\right)$ for $\sigma_0 = 0$
V	$\frac{1}{2}\left(v_{wu}^* + \frac{i_s^* + v_{vw}^* i_v}{i_u}\right)$ for $\sigma_0 = 1$	V	$\frac{1}{2}\left(-v_{vw}^* + \frac{i_s^* - v_{wu}^* i_u}{i_v}\right)$ for $\sigma_0 = 1$
III VI	$\frac{1}{2}min\left\{v_{wu}^* + \frac{i_s^* + v_{vw}^* i_v}{i_u}, -v_{vw}^* - \frac{i_s^* + v_{wu}^* i_u}{i_v}\right\}$	III VI	$\frac{1}{2}max\left\{v_{wu}^* - \frac{i_s^* - v_{vw}^* i_v}{i_u}, -v_{vw}^* + \frac{i_s^* - v_{wu}^* i_u}{i_v}\right\}$

$$\sigma_0 = sign\left\{\left|i_s\left(v_{w,max}\right) - i_s\left(0\right)\right| - \left|i_s\left(v_{w,min}\right) - i_s\left(0\right)\right|\right\}$$

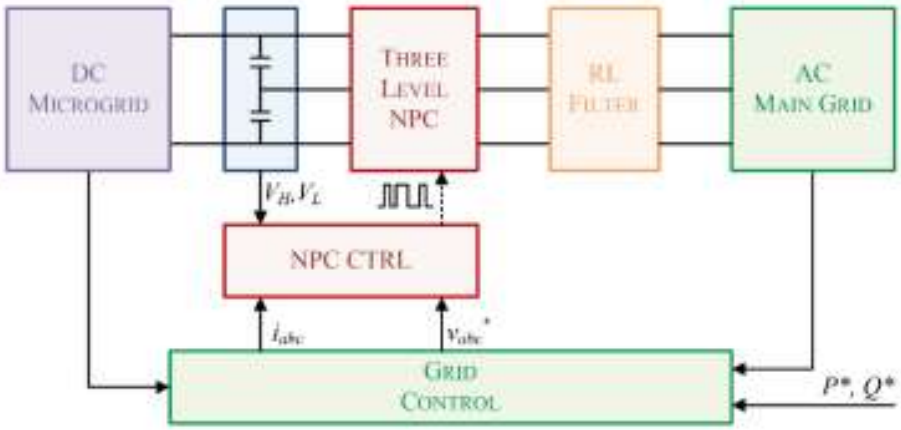

Fig. 9. Simulation set-up.

5. Simulations

In order to verify the performances achievable by means of both Hysteresis and P-based NPC controls, a simulation study has been carried out in the Matlab-Simulink environment. Apart from the proposed Hysteresis and P-based NPC controls, simulations regard also the implementation of the conventional MSVM for comparison purposes [52]. Reference has been made to the simulation set-up shown in Fig. 9, which consists mainly of a DC microgrid, an NPC and the main AC grid. The DC microgrid is assumed to be made up of a number of distributed generators and loads, whose overall residual power is assumed not to exceed 30 kW over both generation and loading periods. The Point of Common Coupling (PCC) between the DC microgrid and the main AC grid is represented by the NPC, which consists mainly of 12 IGBTs and 6 clamping diodes. The overall DC-link voltage has been set to 1500 V, whereas the switching frequency is 10 kHz, the sampling time interval being 100 μs. The NPC minimum pulse width has been considered as well, which has been set to 0.8 μs. The NPC is coupled with the main AC grid through an appropriate RL filter and it is driven by either Hysteresis or P-based NPC control. These controls synthesize the PWM patterns in accordance with both equalization needs and reference chain voltages. The latter are provided by the grid control system in accordance with the desired active and reactive power flows. The MSVM has been considered as well, namely the reference space vector is applied as a weighted sum of the three nearest "base" vectors, while redundant switching states are selected in accordance with DC-link voltage equalization requirements.

Simulations have been performed assuming a constant apparent power of 30 kVA and any angular displacement between AC grid voltages and currents (Φ). This was done in order to check the effectiveness of the proposed control approaches at different power factors and/or active and reactive power levels. Regarding equalization needs, these are represented by any DC-link voltage unbalance, which was initially set to 0.2 p.u. by assuming v_H and v_L equal to 0.6 and 0.4 p.u. respectively.

5.1. Simulation results

Simulations firstly refer to both Hysteresis and P-based NPC control in the case of $\Phi = 0°$, whose corresponding results are depicted from Fig. 10 to Fig. 13. Focusing on both Fig. 10 and Fig. 11 at first, it can be seen that the initial voltage unbalance is quickly and similarly suppressed by both Hysteresis and P-based NPC controls. Particularly, over the equalization process, both control approaches are characterized by almost the same i_M evolution, it being upper-bounded by its maximum threshold. However, DC-link voltage equalization is slightly delayed by P-based NPC control compared to Hysteresis NPC control. This is due to the employment of a proportional regulator, whose dynamic performances are slightly lower than that achievable by means of a hysteresis regulator. As soon as DC-link voltage equalization is almost accomplished, i_M is

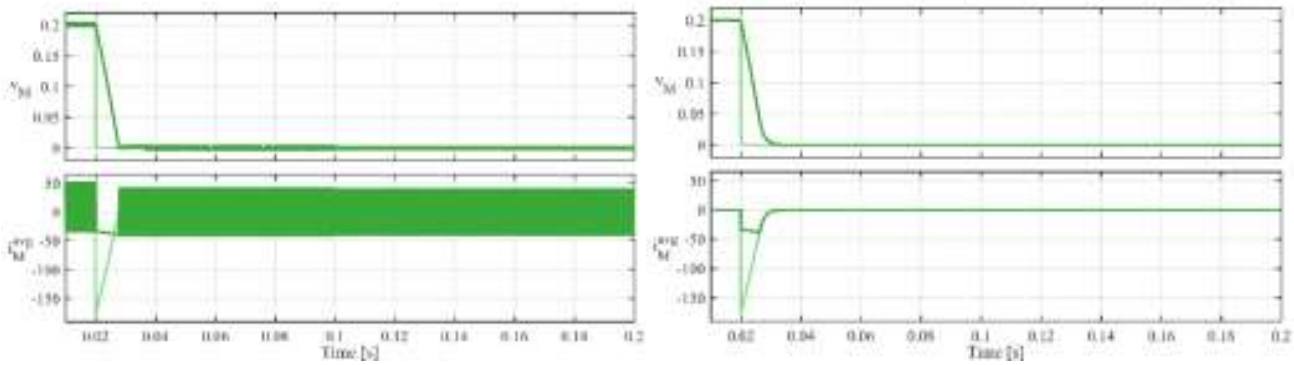

Fig. 10. DC-link voltage and current unbalance evolutions (in p.u. and A respectively) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for $\Phi = 0°$: actual (dark green) and reference (pale green).

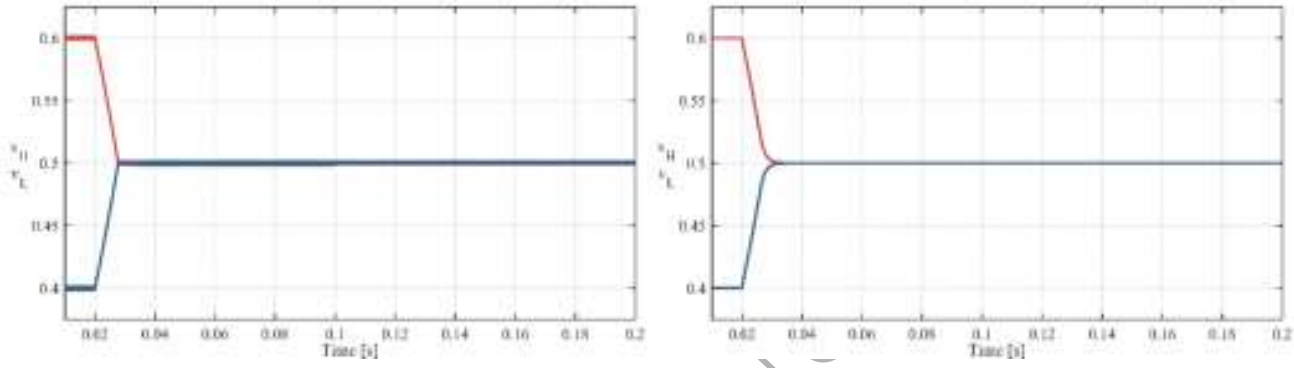

Fig. 11. DC-link voltage evolutions (in p.u.) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for $\Phi = 0°$: high-side capacitor (red) and low-side capacitor (blue).

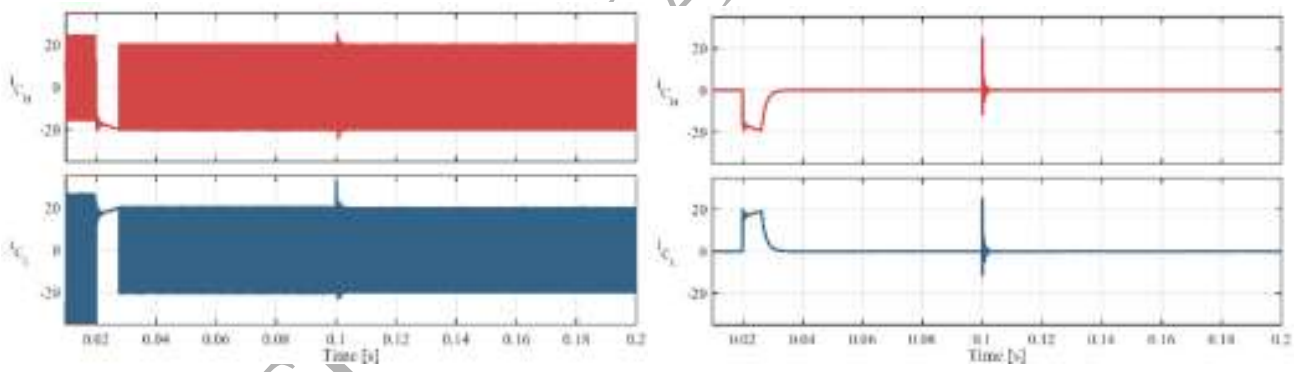

Fig. 12. DC-link capacitor current evolutions (in A) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for $\Phi = 0°$: high-side capacitor (red) and low-side capacitor (blue).

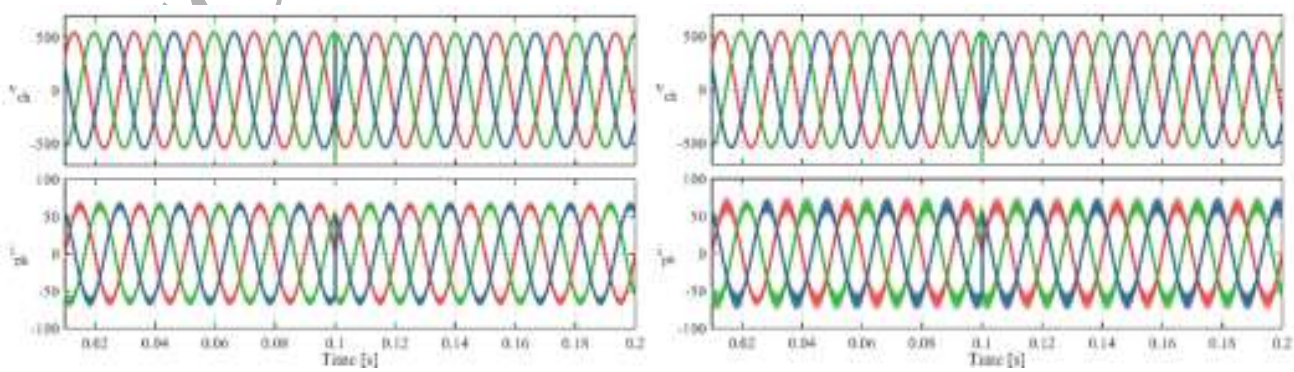

Fig. 13. Chain voltages and phase currents evolutions (in V and A respectively) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for $\Phi = 0°$.

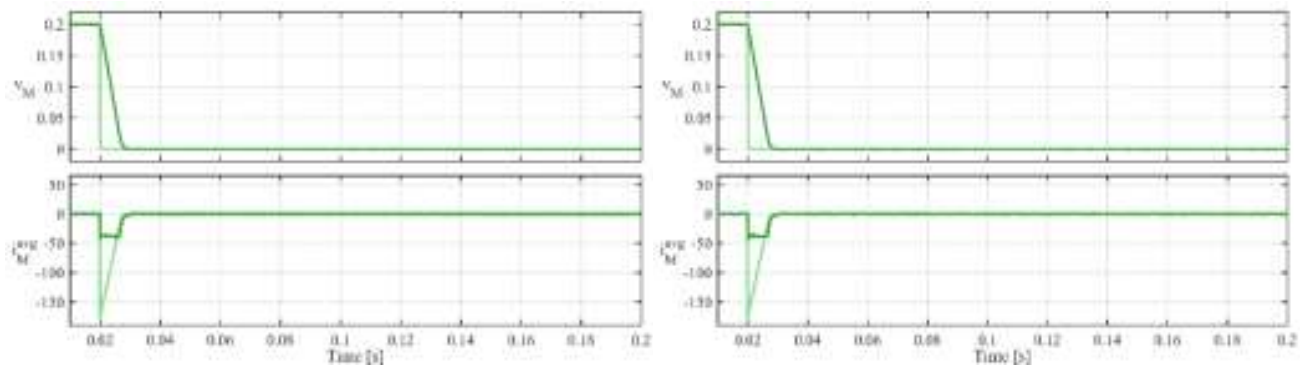

Fig. 14. DC-link voltage and current unbalance evolutions (in p.u. and A respectively) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 0°: actual (dark green) and reference (pale green).

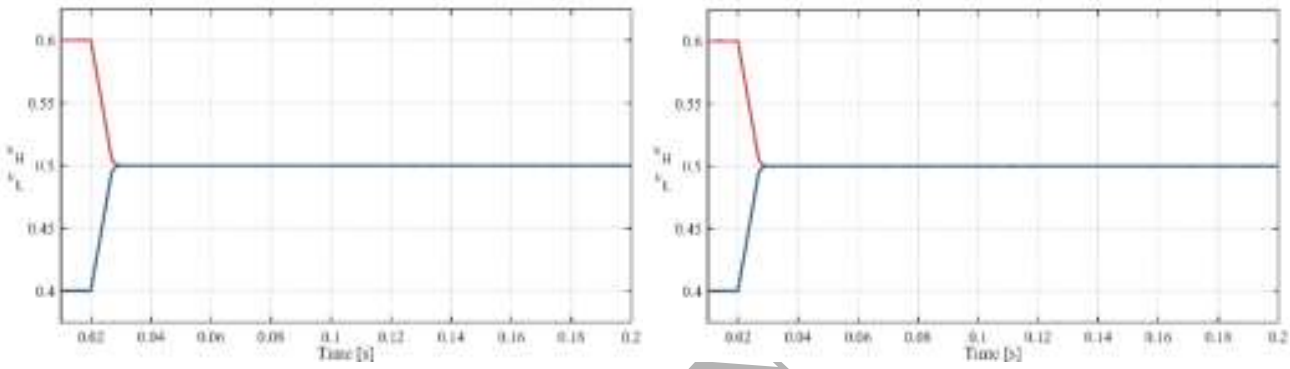

Fig. 15. DC-link voltage evolutions (in p.u.) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 0°: high-side capacitor (red) and low-side capacitor (blue).

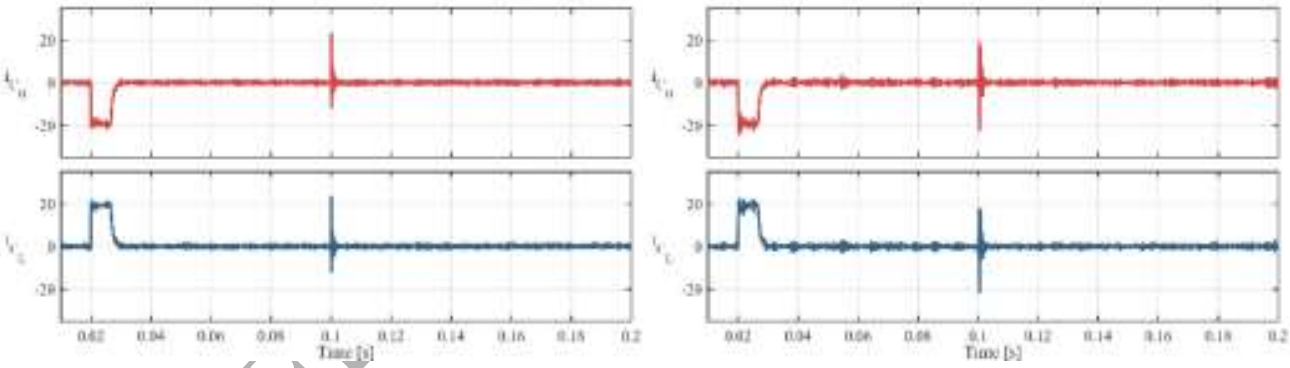

Fig. 16. DC-link capacitor current evolutions (in A) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 0°: high-side capacitor (red) and low-side capacitor (blue).

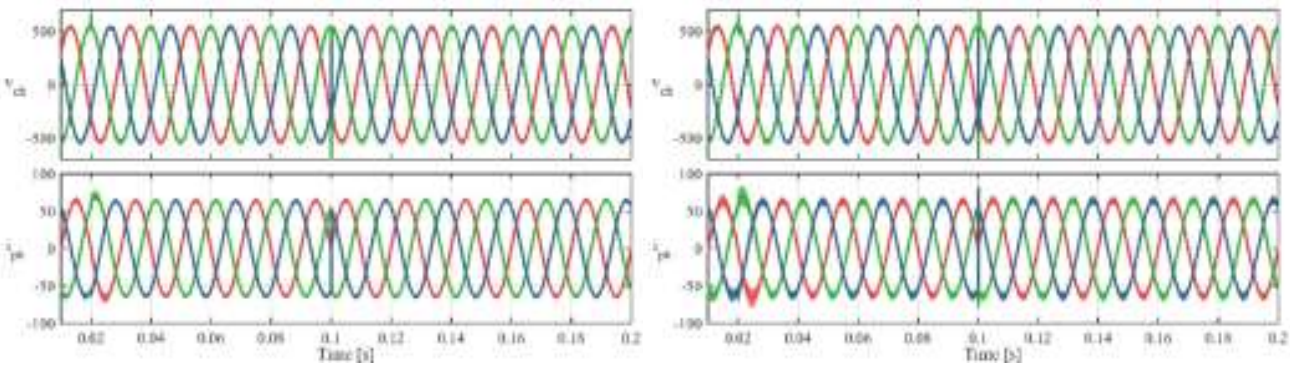

Fig. 17. Chain voltages and phase currents evolutions (in V and A respectively) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 0°.

successfully driven to zero by P-based NPC control, its ripple being almost negligible. Whereas the hysteretic nature of Hysteresis NPC control introduces high frequency ripple on i_M and, consequently, on both DC-link capacitor currents, as shown in Fig. 12. This drawback is avoided appropriately by P-based NPC control due to the more accurate control of DC-link currents, as highlighted by both Fig. 10 and Fig. 12. Consequently, given a maximum current ripple, reduced-size and cheaper DC-link capacitors could be employed as far as P-based NPC control is concerned. Alternatively, switching frequency can be reduced safely, meaning that P-based NPC control seems also well-suited for high-power applications characterized by relatively low switching frequencies. Focusing now on the phase current evolutions depicted in Fig. 13, it can be seen that higher current ripple occurs by P-based NPC control than that achieved by Hysteresis NPC control. This phenomenon is related to the different duty cycles synthesized by the two control approaches. In particular, once achieved, DC-link voltage equalization requires high-side and low-side capacitors to be exploited equally, as in a pure series connection. This goal is well achieved by P-based NPC control, leading to short duty cycles and maximum magnitude of voltage pulses. Hysteresis NPC control however, fully exploits high-side and low-side capacitors alternatively, leading to larger voltage pulses of reduced magnitude compared to P-based NPC control. Nevertheless, it is worth noting that the increased ripple achieved by P-based NPC control on phase currents is quite small if compared to the ripple reduction achieved on capacitor currents, as highlighted by Fig. 12. In order to test the effectiveness of both Hysteresis and P-based NPC controls in preserving DC-link voltage equalization, a power inversion is performed at 0.1s (Φ = 180°), the corresponding results still being shown from Fig. 10 to Fig. 13. It can be seen that some ripple occurs transiently on capacitor currents in both cases, but it does not affect DC-link voltage equalization significantly.

The simulation results achieved by means of MSVM by considering two different switching frequencies (10 and 5 kHz) are depicted from Fig. 14 to Fig. 17. It can be seen that MSVM is able to equalize the DC-link voltage similarly to the proposed Hysteresis and P-based NPC controls. However, MSVM achieves weaker performances in terms of phase current tracking in presence of large DC-link voltages unbalances. On the other hand, a much lower phase current ripple occurs by employing MSVM at 10 kHz compared to both Hysteresis and P-based NPC controls, as highlighted by the comparison between Fig. 13 and Fig. 17. This is due to the suitable exploitation of redundant switching states achieved by MSVM at the cost of an increased number of commutations, as pointed out in Table 9. This reveals that Hysteresis NPC control is characterized by the minimum number of commutations, the corresponding phase current ripple being very similar to that achieved by MSVM at 5 kHz. The weakest performances in terms of phase current ripple are achieved by the P-based NPC control, the corresponding number of commutations being also greater than Hysteresis NPC control. However, P-based NPC control is the best solution in terms of capacitor current ripple minimization, also in comparison with MSVM at both 5 and 10 kHz. The best performances in terms of phase current ripple are achieved by MSVM at 10 kHz, but at the cost of a large number of commutations and, thus, of significant switching losses compared to the other cases.

Different performances are achieved in terms of DC-link voltage equalization for Φ = 120°, whose corresponding results are reported from Fig. 18 to Fig. 25. In particular, Fig. 18 and Fig. 22

Table 9
Average number of commutations per cycle and per switch for HML-PWM, PS-PWM and MSVM in case of Φ = 0°, 180°

Case	HML-PWM (@ 10 kHz)	P-based PWM (@ 10 kHz)	MSVM (@ 10 kHz)	MSVM (@ 5 kHz)
30 kVA , Φ = 0°	16.7	24.3	47.4	23.8
30 kVA , Φ = 180°	16.6	24.9	48.8	24.7

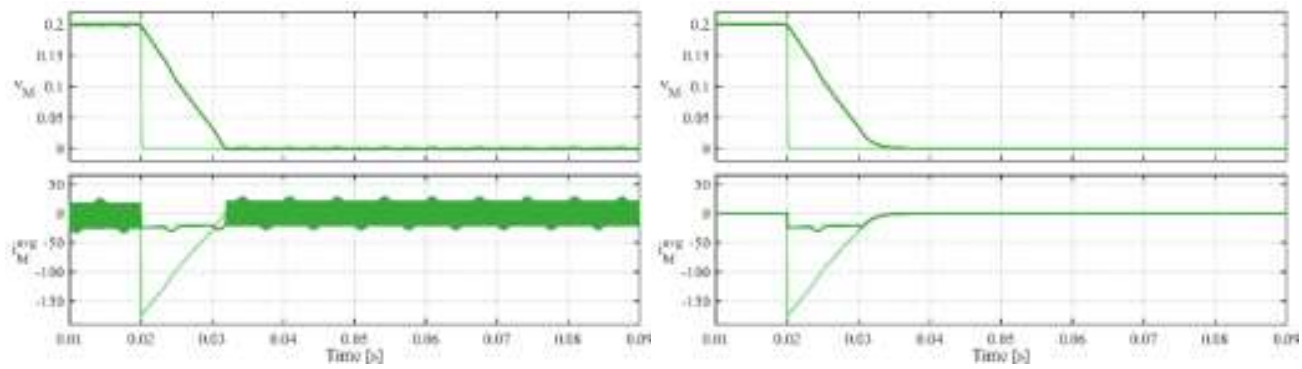

Fig. 18. DC-link voltage and current unbalance evolutions (in p.u. and A respectively) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for Φ = 120°: actual (dark green) and reference (pale green).

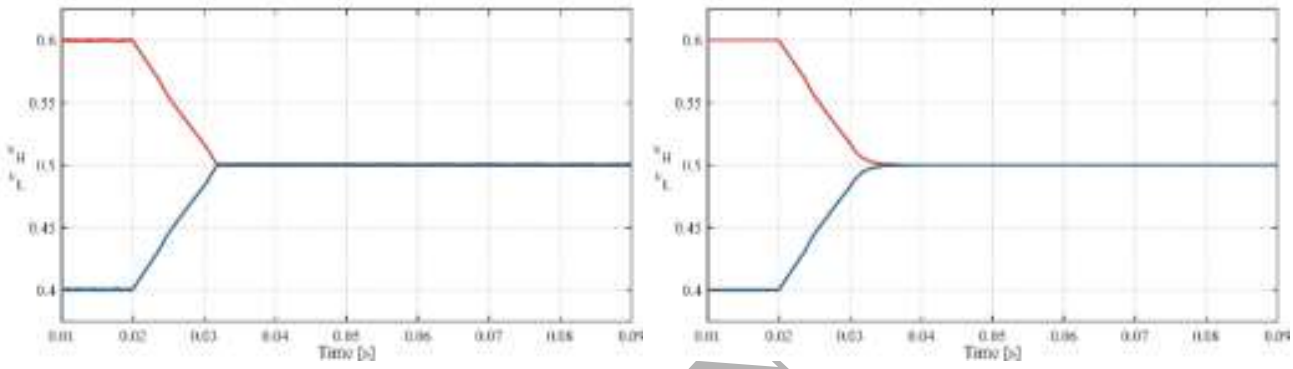

Fig. 19. DC-link voltage evolutions (in p.u.) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for Φ = 120°: high-side capacitor (red) and low-side capacitor (blue).

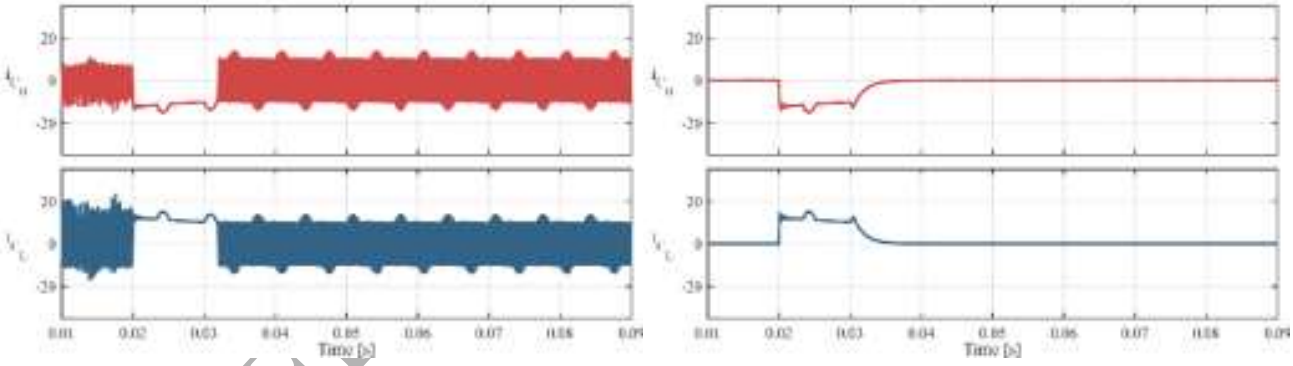

Fig. 20. DC-link capacitor current evolutions (in A) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for Φ = 120°: high-side capacitor (red) and low-side capacitor (blue).

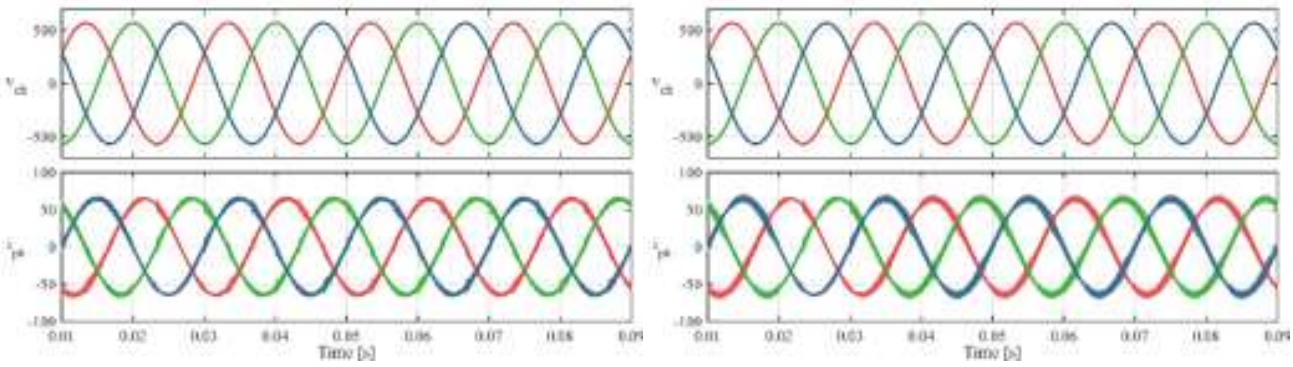

Fig. 21. Chain voltages and phase currents evolutions (in V and A respectively) achieved by Hysteresis NPC control (left) and P-based NPC control (right) for Φ = 120°.

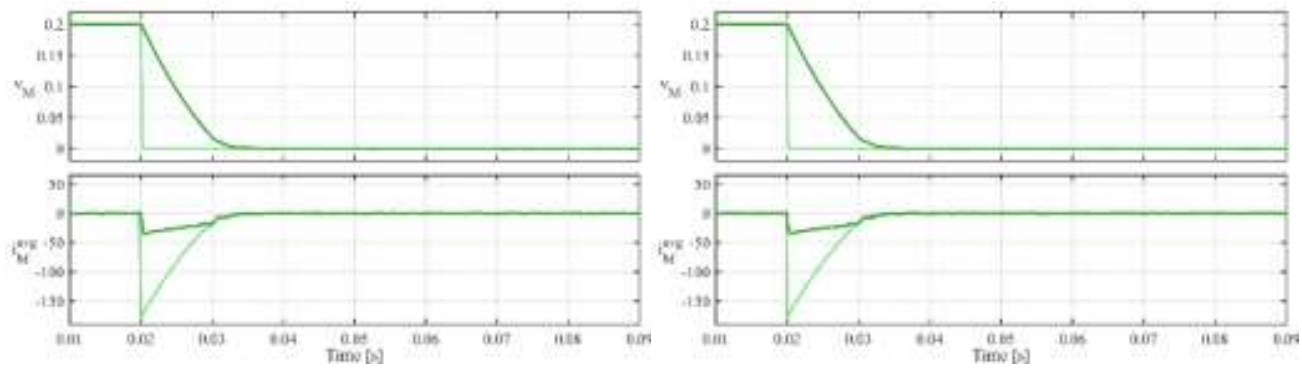

Fig. 22. DC-link voltage and current unbalance evolutions (in p.u. and A respectively) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 120°: actual (dark green) and reference (pale green).

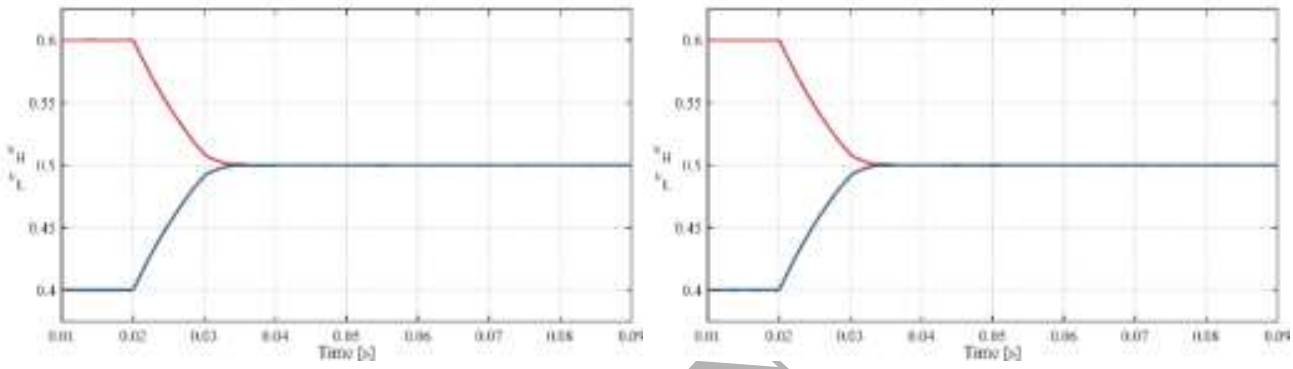

Fig. 23. DC-link voltage evolutions (in p.u.) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 120°: high-side capacitor (red) and low-side capacitor (blue).

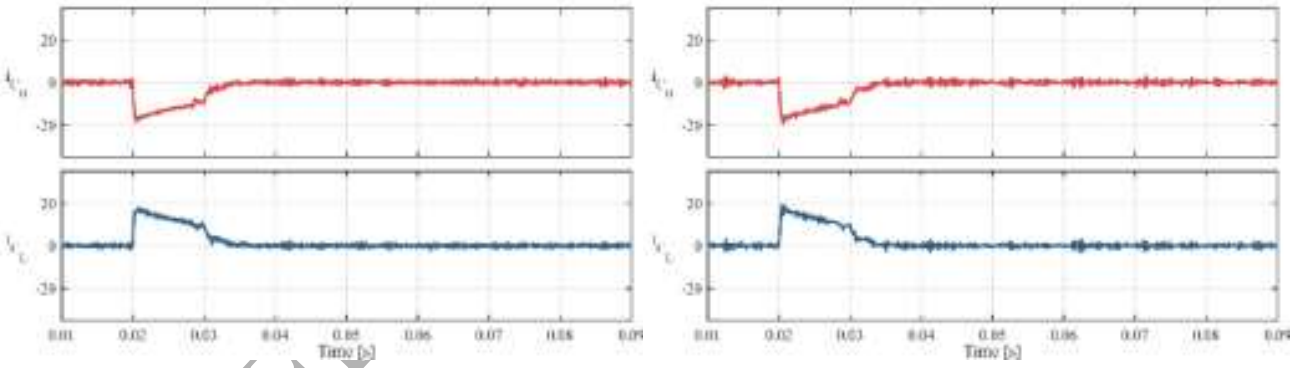

Fig. 24. DC-link capacitor current evolutions (in A) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 120°: high-side capacitor (red) and low-side capacitor (blue).

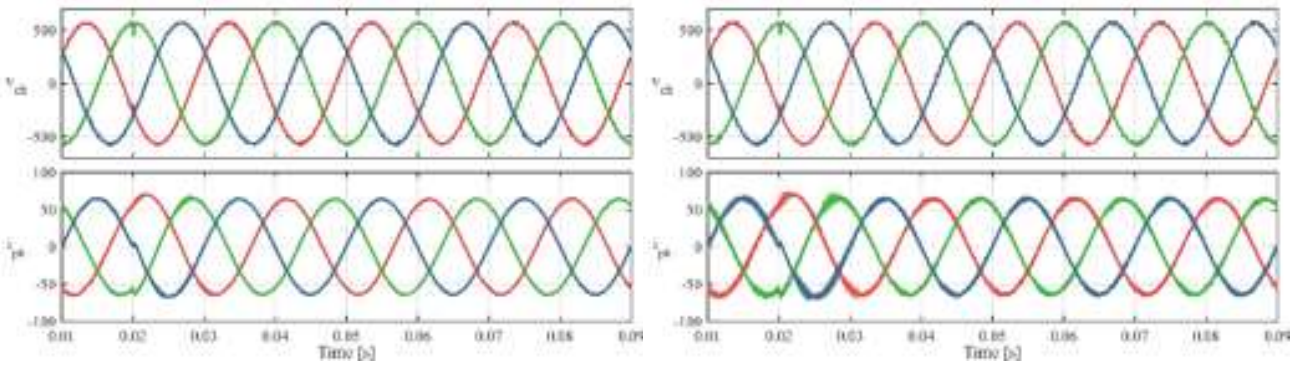

Fig. 25. Chain voltages and phase currents evolutions (in V and A respectively) achieved by MSVM NPC at 10 kHz (left) and 5 kHz (right) for Φ = 120°.

Table 10
Average number of commutations per cycle and per switch for HML-PWM, PS-PWM and MSVM in case of Φ = 120°

Case	HML-PWM (@ 10 kHz)	P-based PWM (@ 10 kHz)	MSVM (@ 10 kHz)	MSVM (@ 5 kHz)
30 kVA , Φ = 120°	33.2	48.9	95.6	48.2

reveal that this poor power factor reduces i_M threshold significantly, leading to a much slower DC-link voltage equalization than that achieved in the previous case. In addition, although current ripple achieved by Hysteresis NPC control is lower than P-based NPC control, it seems irregular, as highlighted in Fig. 21. Despite these drawbacks, DC-link voltage equalization is accomplished successfully also in this case, as shown by both Fig. 19 and Fig. 23. Furthermore, also referring to Table 10, the comparison between the proposed control approaches and the MSVM highlights advantages and drawbacks similar to those pointed out in the case of Φ = 0° and Φ = 180°.

The overall performances achieved by Hysteresis and P-based NPC controls in equalizing DC-link voltages at 30 kVA are resumed from Fig. 26 to Fig. 28, together with those related to MSVM for comparison purposes. Referring to Fig. 26 and Fig. 27 at first, it can be seen that the DC-link voltage equalization time decreases significantly as the active power level increases, it being almost unaffected by power flow direction. Consequently, the weakest equalization performances are achieved when Φ = 90° and Φ = 270°, in correspondence to which the active power provided by the NPC is due to system Joule losses only. The comparison between Fig. 26 and Fig. 27 reveals that MSVM equalization performances are slightly weaker than those achieved by both Hysteresis and P-based NPC controls when Φ approaches 90° and 270°, although DC-link voltage equalization provided by MSVM is faster in correspondence to Φ = 270°.

In order to further corroborate the effectiveness of the proposed NPC control approaches, reference can be made to the Total Harmonic Distortion (THD) of the phase currents, which is determined by taking into account all the harmonic components up to the 40th order, and the capacitor current ripple depicted in Fig. 28. Focusing on THD at first, both Hysteresis and P-based NPC controls enable the achievement of a very good THD compared to that achieved by MSMV

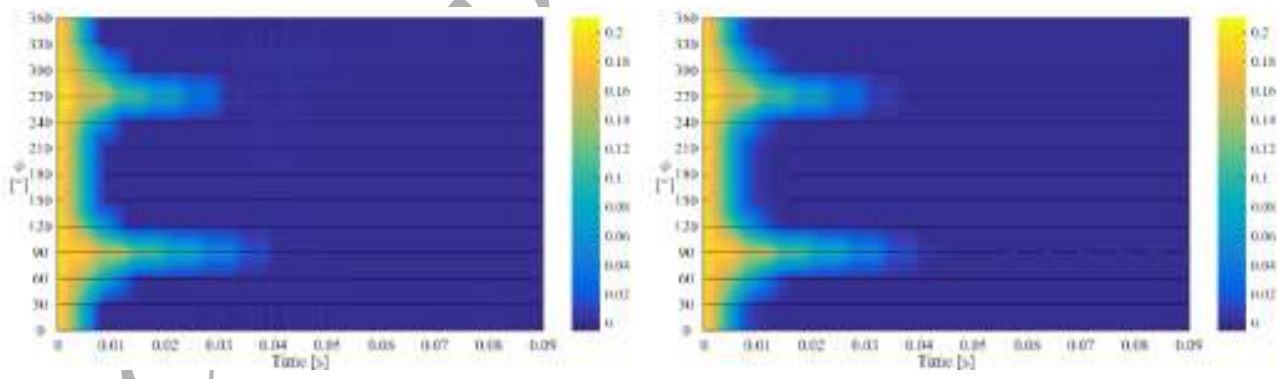

Fig. 26. DC-link voltage unbalance (colormap, in p.u.) achieved by Hysteresis NPC control (left) and P-based NPC control (right).

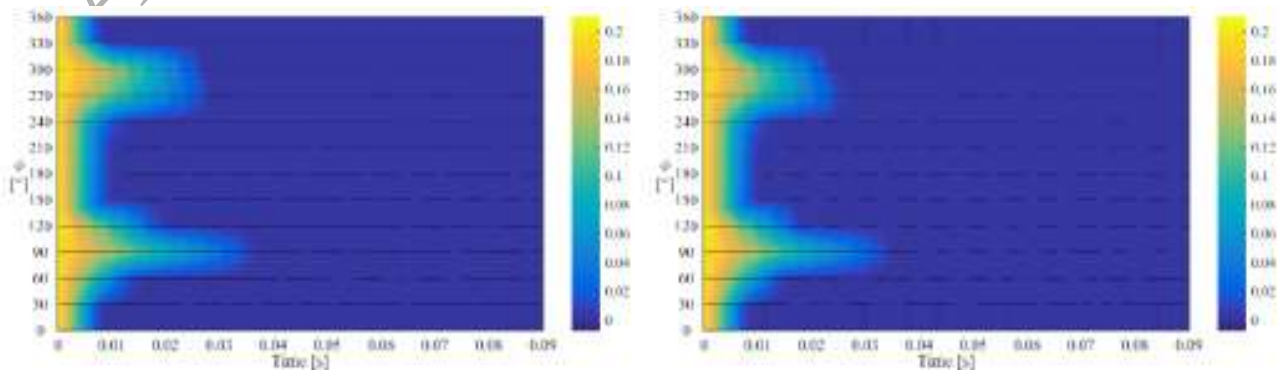

Fig. 27. DC-link voltage unbalance (colormap, in p.u.) achieved by MSVM at 10 kHz (left) and 5 kHz (right).

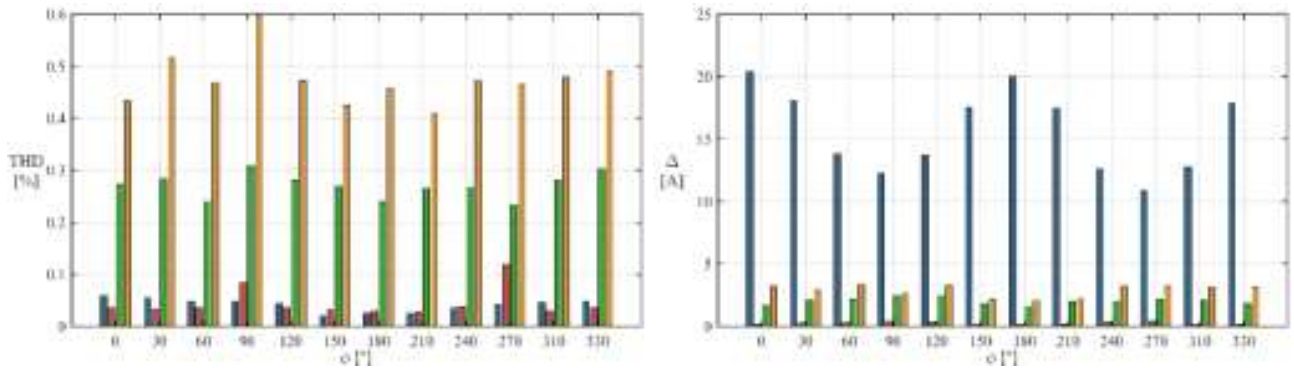

Fig. 28. The THD of phase currents (left) and ripple of capacitor currents (right): hysteresis NPC control (blue), P-based NPC control (red), MSVM at 10 kHz (green) and at 5 kHz (orange).

(at both 5 and 10 kHz). This means that the non-negligible phase current ripple achieved by the P-based NPC control (Fig. 13 and Fig. 21) is characterized by a high-order harmonic content. Much greater THD values are achieved by MSVM, however, they are acceptably low. Different considerations have to be made for capacitor current ripple, namely the weakest performances are achieved by Hysteresis NPC control, as expected. Whereas negligible capacitor current ripple is achieved by the P-based NPC control, even in comparison with MSVM, due to a more accurate DC-link current control.

6. Conclusions

Two different approaches for suppressing DC-link voltage unbalance in three-phase Three-Level Neutral Point-Clamped Converters (NPCs) have been presented in this paper. The Hysteresis NPC control is simple and easy to be implemented, but it inherently introduces high-frequency DC-link voltage and current ripple. Whereas P-based NPC control assures a more accurate DC-link voltage and current regulation at the cost of increased complexity and non-negligible high-frequency ripple on NPC phase currents. The proposed control approaches have been compared to the well-known Multilevel Space Vector Modulation (MSVM) through an extensive simulation study performed in the Matlab-Simulink environment. Based on this, the following concluding remarks can be made:

- both Hysteresis and P-based NPC controls guarantee similar and sometimes better performances than MSVM in equalizing DC-link voltages at different values of angular displacement between AC grid voltages and currents, enabling also a phase current THD significantly lower than MSVM;
- Hysteresis NPC control is the best approach in terms of minimum switching losses;
- P-based NPC control assures minimum DC-link voltage and current ripple.

Consequently, both the proposed Hysteresis and P-based NPC controls represent valid alternatives to conventional NPC controls, especially in terms of DC-link capacitor current ripple or switching losses minimization.

Appendix

All the symbols employed in the paper and their meaning are summed up in Table A1.

Table A1
Paper symbols and meanings.

Symbol	*Meaning*
V_H (V_L)	High-side (low-side) DC-link capacitor voltage
V_x	Terminal voltage of the phase x
H, M, L	Leg states
$S_x^{(1)}$, $S_x^{(2)}$, $S_x^{(3)}$,$S_x^{(4)}$	Switching states of the leg x
v_x	Per unit terminal voltage of the phase x
δ_H (δ_L)	Duty cycle of the H (L) leg state
$\{\alpha,\beta,\gamma\}$	Duty cycles of the phases $\{a,b,c\}$
$\{a,b,c\}$	Phase terminal indexes
v_H (v_L)	Per unit high-side (low-side) DC-link capacitor voltage
v_{ab}, v_{bc}, v_{ca}	Per-unit chain voltages
i_H, i_L	DC-link currents
i_a, i_b, i_c	Phase currents
i_{DC}	DC current
C	Capacitance of each DC-link capacitor
V_M (i_M)	Voltage (Current) unbalance
σ_v (σ_i)	Voltage (Current) sector
$\{u,v,w\}$	Alternative indexes of phase terminals
s_{ab}^*,s_{bc}^*,s_{ca}^*	Binary signs of the reference chain voltages
$\{\varphi,\psi,\xi\}$	Duty cycles of the phases $\{u,v,w\}$
$\{s_u,s_v,s_w\}$	Binary signs of the actual phase currents
ε	Binary signal synthesized by the hysteresis regulator
i_p	Equivalent power current
i_s	Auxiliary current
k	Gain of the DC-link voltage proportional regulator
f_{DC}	Bandwidth of the DC-link voltage unbalance control loop
Φ	Angular displacement between AC grid voltages and currents

References

[1] B. Wu, *High-Power Converters and AC Drives*. Wiley, 2006.

[2] A. Nabae, I. Takahashi, and H. Akagi, “A New Neutral-Point-Clamped PWM Inverter,” *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, “Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[4] R. Teichmann and S. Bernet, “A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 855–865, May 2005.

[5] K. Arulkumar, D. Vijayakumar, and K. Palanisamy, “Modeling and control strategy of three phase neutral point clamped multilevel PV inverter connected to the grid,” *J. Build. Eng.*, Jun. 2015.

[6] J.-S. Lee, K.-B. Lee, and F. Blaabjerg, “Open-Switch Fault Detection Method of a Back-to-Back Converter Using NPC Topology for Wind Turbine Systems,” *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 325–335, Jan. 2015.

[7] A. Etxeberria, I. Vechiu, S. Baudoin, H. Camblong, and S. Kreckelbergh, “Control of a Vanadium Redox Battery and supercapacitor using a Three-Level Neutral Point Clamped converter,” *J. Power Sources*, vol. 248, pp. 1170–1176, Feb. 2014.

[8] A. Etxeberria, I. Vechiu, H. Camblong, S. Kreckelbergh, and S. Bacha, "Operational limits of a three level neutral point clamped converter used for controlling a hybrid energy storage system," *Energy Convers. Manag.*, vol. 79, pp. 97–103, Mar. 2014.

[9] S. D. G. Jayasinghe, D. M. Vilathgamuwa, and U. K. Madawala, "A new method of interfacing battery/supercapacitor energy storage systems for distributed energy sources," in *Proc. of 9th International Power Engineering Conference (IPEC 2010)*, Singapore (Singapore), 2010, pp. 1211–1216.

[10] M. Porru, "Management and Control of Energy Storage Systems for Stationary and Automotive Applications," PhD Dissertation, Department of Electrical and Electronic Engineering, University of Cagliari, Italy, 2015.

[11] A. Choudhury, P. Pillay, and S. S. Williamson, "Comparative Analysis Between Two-Level and Three-Level DC/AC Electric Vehicle Traction Inverters Using a Novel DC-Link Voltage Balancing Algorithm," *Emerg. Sel. Top. Power Electron. IEEE J. Of*, vol. 2, no. 3, pp. 529–540, Sep. 2014.

[12] S. Rivera, B. Wu, S. Kouro, V. Yaramasu, and J. Wang, "Electric Vehicle Charging Station Using a Neutral Point Clamped Converter With Bipolar DC Bus," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 1999–2009, Apr. 2015.

[13] S. Srikanthan and M. K. Mishra, "DC Capacitor Voltage Equalization in Neutral Clamped Inverters for DSTATCOM Application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.

[14] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM With DC-Link Capacitor Voltage Balancing Control for Diode-Clamped Multilevel Converter Based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.

[15] M. G. Molina, P. E. Mercado, and E. H. Watanabe, "Analysis of integrated STATCOM-SMES based on three-phase three-level multi-pulse voltage source inverter for high power utility applications," *J. Frankl. Inst.*, vol. 348, no. 9, pp. 2350–2377, Nov. 2011.

[16] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[17] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Convers. Manag.*, vol. 52, no. 2, pp. 1114–1128, Feb. 2011.

[18] A. H. Bhat and N. Langer, "Capacitor Voltage Balancing of Three-Phase Neutral-Point-Clamped Rectifier Using Modified Reference Vector," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 561–568, Feb. 2014.

[19] G. I. Orfanoudakis, M. A. Yuratich, and S. M. Sharkh, "Nearest-Vector Modulation Strategies With Minimum Amplitude of Low-Frequency Neutral-Point Voltage Oscillations for the Neutral-Point-Clamped Converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4485–4499, Oct. 2013.

[20] K. S. Gopalakrishnan and G. Narayanan, "Space vector based modulation scheme for reducing capacitor RMS current in three-level diode-clamped inverter," *Electr. Power Syst. Res.*, vol. 117, pp. 1–13, Dec. 2014.

[21] A. Das, K. Sivakumar, R. Ramchand, C. Patel, and K. Gopakumar, "A Pulsewidth Modulated Control of Induction Motor Drive Using Multilevel 12-Sided Polygonal Voltage Space Vectors," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2441–2449, Jul. 2009.

[22] A. Edpuganti and A. K. Rathore, "A Survey of Low Switching Frequency Modulation Techniques for Medium-Voltage Multilevel Converters," *IEEE Trans. Ind. Appl.*, vol. PP, no. 99, pp. 1–1, 2015.

[23] S. Khomfoi and L. M. Tolbert, "Multilevel Power Converters," in *Power Electronics Handbook*, Butterworth-Heinemann, Elsevier, 2011, pp. 455–486.

[24] A. Damiano, M. Marchesoni, I. Marongiu, and A. Taffone, "Optimization of harmonic performances in multilevel converter structures," in *Proc. of 6th IEEE International Symposium on Industrial Electronics (ISIE 1997)*, Guimaraes (Portugal), 1997, vol. 2, pp. 341–346 vol.2.

[25] U.-M. Choi, J.-S. Lee, and K.-B. Lee, "New Modulation Strategy to Balance the Neutral-Point Voltage for Three-Level Neutral-Clamped Inverter Systems," *IEEE Trans. Energy Convers.*, vol. 29, no. 1, pp. 91–100, Mar. 2014.

[26] R. Portillo, S. Vazquez, J. I. Leon, M. M. Prats, and L. G. Franquelo, "Model Based Adaptive Direct Power Control for Three-Level NPC Converters," *IEEE Trans. Ind. Inform.*, vol. 9, no. 2, pp. 1148–1157, May 2013.

[27] R. M. Tallam, R. Naik, and T. A. Nondahl, "A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1734–1743, Nov. 2005.

[28] J. Shen, S. Schroder, B. Duro, and R. Roesner, "A Neutral-Point Balancing Controller for a Three-Level Inverter With Full Power-Factor Range and Low Distortion," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 138–148, Jan. 2013.

[29] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[30] R. W. Menzies, P. Steimer, and J. K. Steinke, "Five-level GTO inverters for large induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 30, no. 4, pp. 938–944, Jul. 1994.

[31] S. Halasz, G. Csonka, and A. A. M. Hassan, "Sinusoidal PWM techniques with additional zero-sequence harmonics," in *, 20th International Conference on Industrial Electronics, Control and Instrumentation, 1994. IECON '94*, 1994, vol. 1, pp. 85–90 vol.1.

[32] D. G. Holmes, "The significance of zero space vector placement for carrier-based PWM schemes," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1122–1129, Sep. 1996.

[33] H. S. Patel and R. G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I–Harmonic Elimination," *IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 310–317, May 1973.

[34] H. S. Patel and R. G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part II — Voltage Control Techniques," *IEEE Trans. Ind. Appl.*, vol. IA-10, no. 5, pp. 666–673, Sep. 1974.

[35] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.

[36] J. Napoles, J. I. Leon, R. Portillo, L. G. Franquelo, and M. A. Aguirre, "Selective Harmonic Mitigation Technique for High-Power Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2315–2323, Jul. 2010.

[37] Y. Zhang, Z. Zhao, and J. Zhu, "A Hybrid PWM Applied to High-Power Three-Level Inverter-Fed Induction-Motor Drives," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3409–3420, Aug. 2011.

[38] S. Sirisukprasert, J.-S. Lai, and T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 875–881, Aug. 2002.

[39] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "Control of a multilevel converter using resultant theory," *IEEE Trans. Control Syst. Technol.*, vol. 11, no. 3, pp. 345–354, May 2003.

[40] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "A new approach to solving the harmonic elimination equations for a multilevel converter," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003.*, 2003, vol. 1, pp. 640–647 vol.1.

[41] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "A complete solution to the harmonic elimination problem," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 491–499, Mar. 2004.

[42] C. Xia, H. Shao, Y. Zhang, and X. He, "Adjustable Proportional Hybrid SVPWM Strategy for Neutral-Point-Clamped Three-Level Inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4234–4242, Oct. 2013.

[43] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," *IEEE Power Electron. Lett.*, vol. 2, no. 1, pp. 11–15, Mar. 2004.

[44] K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga, and T. Kume, "A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector," *IEEE Trans. Ind. Appl.*, vol. 38, no. 6, pp. 1572–1580, Nov. 2002.

[45] F. Umbría, F. Gordillo, F. Gómez-Estern, F. Salas, R. C. Portillo, and S. Vázquez, "Voltage balancing in three-level neutral-point-clamped converters via Luenberger observer," *Control Eng. Pract.*, vol. 25, pp. 36–44, Apr. 2014.

[46] C. Bharatiraja, S. Jeevananthan, J. L. Munda, and R. Latha, "Improved SVPWM vector selection approaches in OVM region to reduce common-mode voltage for three-level neutral point clamped inverter," *Int. J. Electr. Power Energy Syst.*, vol. 79, pp. 285–297, Luglio 2016.

[47] H. L. Liu, N. S. Choi, and G. H. Cho, "DSP based space vector PWM for three-level inverter with DC-link voltage balancing," in *International Conference on Industrial Electronics, Control and Instrumentation, 1991. Proceedings. IECON '91*, 1991, pp. 197–203 vol.1.

[48] G. Sinha and T. A. Lipo, "A new modulation strategy for improved DC bus utilization in hard and soft switched multilevel inverters," in *23rd International Conference on Industrial Electronics, Control and Instrumentation, 1997. IECON 97*, 1997, vol. 2, pp. 670–675 vol.2.

[49] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[50] J. Shen, S. Schröder, R. Rösner, and S. El-Barbari, "A Comprehensive Study of Neutral-Point Self-Balancing Effect in Neutral-Point-Clamped Three-Level Inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3084–3095, Nov. 2011.

[51] R. Stala, "A Natural DC-Link Voltage Balancing of Diode-Clamped Inverters in Parallel Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5008–5018, Nov. 2013.

[52] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[53] C. B. Jacobina, A. M. N. Lima, E. R. C. da Silva, R. N. C. Alves, and P. F. Seixas, "Digital scalar pulse-width modulation: a simple approach to introduce nonsinusoidal modulating waveforms," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 351–359, May 2001.

[54] E. R. C. da Silva, E. C. dos Santos, and C. B. Jacobina, "Pulsewidth Modulation Strategies," *IEEE Ind. Electron. Mag.*, vol. 5, no. 2, pp. 37–45, Jun. 2011.

[55] A. Damiano, I. Marongiu, M. Porru, and A. Serpi, "A suitable PWM for DC-link voltage equalization of Three-Level Neutral-Point Clamped Converters," in *Proc. of 39th Annual Conference of the IEEE Industrial Electronics Society (IECON 2013)*, Vienna (Austria), 2013, pp. 328–333.

[56] M. Porru, A. Serpi, I. Marongiu, and A. Damiano, "An improved DC-link voltage equalization for Three-Level Neutral-Point Clamped converters," in *Proc. of 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME 2014)*, Grenoble (France), 2014, pp. 1–4.

[57] M. Porru, A. Serpi, I. Marongiu, and A. Damiano, "A novel DC-link voltage and current control algorithm for Neutral-Point-Clamped converters," in *Proc. of 40th Annual Conference of the IEEE Industrial Electronics Society (IECON 2014)*, Dallas (USA), 2014, pp. 4521–4527.